# 1. 特性

- 输出配置
  - 立体声 2.0: 2 × 32W (8Ω, 24V, THD + N = 10%)
  - 立体声 2.0: 2 × 26W (8Ω, 21V, THD + N = 1%)
- 供电电压范围
  - PVDD: 4.5V – 26.4V
  - DVDD: 1.8V 或者 3.3V
- 静态功耗
  - 37mA at PVDD=12V
- 音频性能指标
  - THD+N ≤ 0.02% at 1W, 1kHz
  - SNR ≥ 107dB (A-weighted)
  - DC offset ≤ 5mV
- 音频输入信号格式
  - 3-wire I2S, LJ,RJ, TDM (无需 MCLK)
  - Fs 支持 32/44.1/48/88.2/96/176.4/192kHz 采样率
  - 支持独立回声消除通道 Sdout
- 音频 DSP 算法
  - 2×15 EQs +3-band DRC+AGL+3*post EQs
  - DPEQ 或者 3D 音效
  - Class H 算法
- 控制模式
  - 支持 I2C 软件配置模式
  - 支持硬件 IO 控制模式，无需 I2C 寄存器控制
  - 两个通道可独立开启或者关闭
  - 最多支持 6 个 I2C 地址
- 保护功能
  - 过流/过压/过温/欠压/直流保护
  - 过流保护门限 6.5A
  - PVDD 掉电检测自动关闭
  - 支持系统级热管理保护
- 调音及系统集成
  - 一站式 GUI 调音软件 ASATP，驱动级整体解决方案
  - 支持上位机一键生成配置文件

# 2. 应用

- 专业音响设备
- 智能音箱
- 条形音响
- 电视
- 笔记本电脑
- 会议系统

# 3. 说明

AU6825 是一款数字输入型，立体声，高效的音频 class D 功率放大器，其最大输出功率可达 2×32W 或者 1× 64W。

AU6825 采用创新的调制模式，可以有效降低静态功耗，如何配合外部 boost 电路，可以实现 class H 算法，从而有效提升电池供电应用的续航时间。AU6825 内部集成 32 位的高精度音频 DSP，提供包括 2×15 个均衡器，3 段 DRC 等调音算法，此外，为了进一步增强小音量下的低音表现，AU6825 还支持动态低音增强算法。针对电视应用场景，AU6825 也提供有 3D 音效算法。AU6825 内部 DSP 处理带宽最大支持 96kHz (192kHz 采样率)。

在音质表现方面，AU6825 的 THD+N 指标可以达到 0.03% 以下的水平，此外极低的直流偏置电压是的 AU6825 在开机关机 pop 音方面具备极其出色的性能。此外，AU6825 还集成 PVDD 掉电检测电路，可以在 PVDD 突然掉电情况下通知控制器或者芯片可以自动关闭，防止掉电 pop 音。

作为一款中大功率音频功率放大器，AU6825 在热管理方面支持四档过问报警和过温度关断保护，此外该芯片温度可以通过寄存器连续输出，方便系统做整体热管理。在喇叭保护方面，AU6825 还支持过流/过压/欠压/直流保护等。

AU6825 支持 QFN-32 封装，无需散热片，其额定温度范围为 - 40° C 至+85° C。有关订购信息，请参见表 1.

THD+N performance @ 1W, 10uH=0.68uF, 6ohm

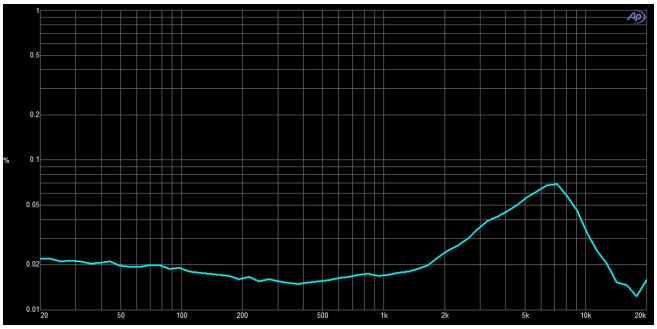


Table 1 lists the order information.

## Table 1.Order Information

| ORDER NUMBER (See Note 1) | PART NUMBER | CH (#) | PACKAGE | MARKING INFO. (See Note 2 and Note 3) | Output Power (W) | Digital Input | PVDD (TYP) (V) | OPERATING TEMP (°C) | PACKAGE OPTION |
|---|---|---|---|---|---|---|---|---|---|
| AU6825AQFN32 | AU6825 | 2 | QFN-32 | AU6825 | 2 × 32W | Yes | 26.4V | -40-85 | 4000 |

Devices can be ordered via the following two ways:

1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note:



# 4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration of the AU6825 .

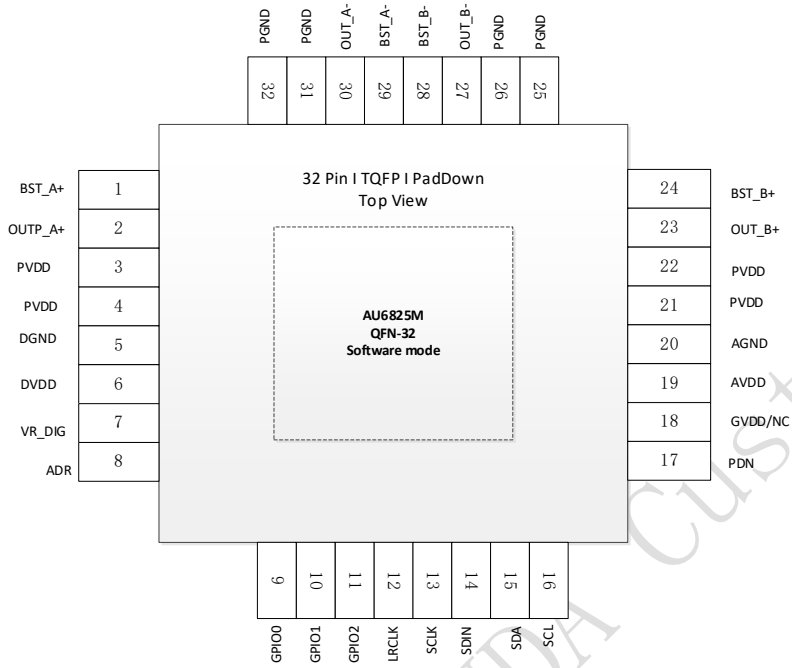



Figure 1. Pin Configuration

Table 2 lists the pin functions

Table 2. Pin Functions

| NAME | POSITION | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| DGND | 5 | P | Digital ground |
| DVDD | 6 | P | 3.3V or 1.8V digital power supply |
| VR_DIG | 7 | P | Internally regulated 1.8V digital supply voltage. This pin must not be used to drive external devices. |
| ADR | 8 | AI | A table of resistor value (Pull down to GND) will decide device I2C address. Support up to 6 addresses. |
| GPIO0 | 9 | DI/O | GPIO0. |
| GPIO1 | 10 | DI/O | GPIO1. |
| GPIO2 | 11 | DI/O | GPIO2. |
| LRCLK | 12 | DI | Word select clock for the digital signal that is active on the serial port's input data line. In I²S, LJ, and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary. |
| SCLK | 13 | DI | Bit clock for the digital signal that is active on the input data line of the serial data port. |
| SDIN | 14 | DI | Data line to the serial data port |
| SDA | 15 | DI/O | I²C serial control data interface input/output |
| SCL | 16 | DI | I²C serial control clock input |
| $\overline{\text{PDN}}$ | 17 | DI | Power-down, active-low. $\overline{\text{PDN}}$ places the amplifier in Shutdown, and turns off all internal regulators. Low—Power down device; High—Enable device. |
| GVDD | 18 | P | GVDD |
| AVDD | 19 | P | AVDD |
| AGND | 20 | P | Analog ground |

| NAME | POSITION | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| PVDD | 3,4,21,22 | P | PVDD voltage input |
| PGND | 25,26,31,32 | P | Ground reference for power device circuitry. Connect this pin to system ground. |
| OUT_B+ | 23 | O | Positive pin for differential speaker amplifier output B+ |
| BST_B+ | 24 | P | Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+ |
| OUT_B– | 27 | O | Negative pin for differential speaker amplifier output B |
| BST_B– | 28 | P | Connection point for the OUT_B– bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B– |
| BST_A– | 29 | P | Connection point for the OUT_A– bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A– |
| OUT_A– | 30 | O | Negative pin for differential speaker amplifier output A– |
| BST_A+ | 1 | P | Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+ |
| OUT_A+ | 2 | O | Positive pin for differential speaker amplifier output A+ |
| PowerPAD | | P | Connect to the system ground |

Note: AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0V)

# 5. SPECIFICATIONS

## 5.1 ABSOLUTE MAXIMUM RATINGS

Table 3 lists the absolute maximum ratings of the AU6825 . Free-air room temperature 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

| PARAMETER | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| Voltage | Low-voltage digital supply, DVDD | –0.3 | 3.9 | V |
| | PVDD supply, PVDD | –0.3 | 30 | |
| | DVDD referenced digital inputs(2), $V_{I(DigIn)}$ | –0.3 | $V_{DVDD}$ + 0.5 | |
| | Voltage at speaker output pins, $V_{I(SPK\_OUTxx)}$ | –0.3 | 32 | |
| Temperature | Ambient operating, $T_A$ | –25 | 85 | °C |
| | Storage, $T_{stg}$ | –40 | 125 | |

Note 1: Stresses beyond those listed under Table 3 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 5. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SCL, SDA, SDIN, and $\overline{\text{PDN}}$.

## 5.2 ESD RATINGS

Table 4 lists the ESD ratings of the AU6825 .

Table 4. ESD Ratings

| PARAMETER | SYMBOL | DESCRIPTION | VALUE | UNITS |
|---|---|---|---|---|
| Electrostatic Discharge | $V_{(ESD)}$ | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 RECOMMENDEDOPERATING CONDITIONS

Table 5 lists the recommended operating conditions for the AU6825 . Over operating free-air temperature range, unless otherwise noted.

Table 5. Recommended Operating Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Power Supply Inputs | $V_{(POWER)}$ | DVDD | 1.65 | | 3.63 | V |
| | | PVDD | 4.5 | | 26.4 | |
| Minimum Speaker Load | $R_{SPK}$ | BTL Mode (4.5V ≤ PVDD ≤ 26.4V) | $VOUT_{PEAK}$ / $OCE_{THRES}$ | 4.5 | | Ω |
| Minimum Speaker Load | $R_{SPK}$ | PBTL Mode (4.5V ≤ PVDD ≤ 26.4V) | $VOUT_{PEAK}$ / (2 × $OCE_{THRES}$) | 2.2 | | Ω |
| Minimum Inductor Value in LC Filter under Short-Circuit Condition | $L_{OUT}$ | | 1 | 4.7 | | μH |

Note: The minimal speaker load is limited by OCE threshold. If output peak current < 6.5A, AU6825 also supports lower speaker load with high PVDD. For BTL, the OCE threshold is 5A (typical); For PBTL, the OCE threshold is 13A (typical). The minimal speaker load depends on the output peak voltage.

## 5.4 THERMAL INFORMATION

Table 6 lists the thermal information for the AU6825 .

Table 6. Thermal Information

| PARAMETER | SYMBOL | QFN-32 | UNITS |
|---|---|---|---|
| Junction-to-Ambient Thermal Resistance | $R_{\theta JA}$ | 29.8 | °C/W |
| Junction-to-Case (Top) Thermal Resistance | $R_{\theta JC\ (top)}$ | 12.9 | °C/W |
| Junction-to-Board Thermal Resistance | $R_{\theta JB}$ | 9.9 | °C/W |
| Junction-to-Top Characterization Parameter | $\psi_{JT}$ | 0.3 | °C/W |
| Junction-to-Board Characterization Parameter | $\psi_{JB}$ | 9.6 | °C/W |
| Junction-to-Case (Bottom) Thermal Resistance | $R_{\theta JC\ (bot)}$ | — | °C/W |



## 5.5 ELECTRICAL CHARACTERISTICS

Table 7 lists the electrical characteristics of the AU6825 . Free-air room temperature 25°C, unless otherwise noted.

Table 7. Electrical Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DIGITAL I/O | | | | | | |
| Input Logic High Current Level for DVDD Referenced Digital Input Pins | $\|I_{IH}\|$ | $V_{IL(Digin)} = V_{DVDD}$ | | | 10 | μA |
| Input Logic Low Current Level for DVDD Referenced Digital Input Pins | $\|I_{IL}\|$ | $V_{IL(Digin)} = 0V$ | | | -10 | μA |
| Input Logic High Threshold for DVDD Referenced Digital Inputs | $V_{IH(Digin)}$ | | 70% | | | $V_{DVDD}$ |
| Input Logic Low Threshold for DVDD Referenced Digital Inputs | $V_{IL(Digin)}$ | | | | 30% | $V_{DVDD}$ |
| Output Logic High Voltage Level | $V_{OH(Digin)}$ | $I_{OH}$ = 2mA | 80% | | | $V_{DVDD}$ |
| Output Logic Low Voltage Level | $V_{OL(Digin)}$ | $I_{OH}$ = -2mA | | | 20% | $V_{DVDD}$ |
| $I^2C$ CONTROL PORT | | | | | | |
| Allowable Load Capacitance for Each $I^2C$ Line | $C_{L(I2C)}$ | | | | 400 | pF |
| Support SCL Frequency | $f_{SCL(fast)}$ | No wait states, fast mode | | | 400 | kHz |
| Support SCL Frequency | $f_{SCL(slow)}$ | No wait states, slow mode | | | 100 | kHz |
| SERIAL AUDIO PORT | | | | | | |
| Required LRCLK/FS to SCLK Rising Edge Delay | $t_{DLY}$ | | 5 | | | ns |
| Allowable SCLK Duty Cycle | $D_{SCLK}$ | | 40% | | 60% | |
| Supported Input Sample Rates | $f_S$ | | 32 | | 192 | kHz |
| Supported SCLK Frequencies | $f_{SCLK}$ | | 32 | | 64 | $f_S$ |
| SCLK Frequency | $f_{SCLK}$ | | | | 24.576 | MHz |
| SPEAKER AMPLIFIER (ALL OUTPUT CONFIGURATIONS) | | | | | | |
| Quiescent Supply Current on DVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, DVDD = 3.3V, Play mode and Hiz | | 17 | | mA |
| Quiescent Supply Current on DVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, DVDD = 3.3V, Sleep mode | | 0.8 | | mA |
| Quiescent Supply Current on DVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, DVDD = 3.3V, Deep Sleep mode | | 0.8 | | mA |
| Quiescent Supply Current on DVDD | $I_{cc}$ | $\overline{PDN}$ = 0V, DVDD = 3.3V, Shutdown mode | | 1.4 | | μA |
| Quiescent Supply Current on PVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, PVDD = 13.5V, LC filter = 10μH + 0.68μF, $F_{sw}$ = 768kHz, BD modulation, Play mode | | 29 | | mA |
| Quiescent Supply Current on PVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, PVDD = 13.5V, LC filter = 22μH + 0.68μF, $F_{sw}$ = 384kHz, 1SPW modulation, Play mode | | 18 | | mA |
| Quiescent Supply Current on PVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, PVDD = 13.5V, Output Hi-Z Mode | | 7 | | mA |
| Quiescent Supply Current on PVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, PVDD = 13.5V, Sleep mode | | 2 | | mA |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Quiescent Supply Current on PVDD | $I_{cc}$ | $\overline{PDN}$ = 2V, PVDD = 13.5V, Deep Sleep mode | | 5 | | μA |
| Turn-Off Time | $t_{off}$ | Excluding volume ramp | | | 10 | ms |
| Programmable Gain | $A_{V(SPK\_AMP)}$ | Value represents the "peak voltage" disregarding clipping due to lower PVDD. Measured at 0dB input (1FS). | 4.87 | | 29.5 | V |
| Amplifier Gain Error | $\Delta A_{V(SPK\_AMP)}$ | Gain = 29.5Vp/FS | | 0.5 | | dB |
| Switching Frequency of the Speaker Amplifier | $f_{SPK\_AMP}$ | | | 260 | | kHz |
| | | | | 768 | | kHz |
| Drain-to-Source on Resistance of the Individual Output MOSFETs | $R_{DS(on)}$ | FET + Metallization | | 100 | | mΩ |
| Over-Current Error Threshold | $OCE_{THRES}$ | OUTxx overcurrent error threshold | | 6.5 | | A |
| PVDD Over Voltage Error Threshold | $OVE_{THRES(PVDD)}$ | | | 28 | | V |
| PVDD Under Voltage Error Threshold | $UVE_{THRES(PVDD)}$ | | | 4.2 | | V |
| Over Temperature Error Threshold | $OTE_{THRES}$ | | | 170 | | °C |
| Over Temperature Error Hysteresis | $OTE_{Hystersis}$ | | | 10 | | °C |
| Over Temperature Warning Level | $OTW_{THRES}$ | Read by register 0x73 bit 3 | | 135 | | °C |
| SPEAKER AMPLIFIER (STEREO BTL) | | | | | | |
| Amplifier Offset Voltage | $\lvert V_{OS} \rvert$ | Measured differentially with zero input data, programmable gain configured with 29.5Vp gain, $V_{PVDD}$ = 12V, BD mode | -5 | | 5 | mV |
| Continuous Output Power (per Channel) | $P_{O(SPK)}$ | $V_{PVDD}$ = 12V, RSPK = 4Ω, f = 1kHz, THD + N = 1% | | 14 | | W |
| | | $V_{PVDD}$ = 12V, RSPK = 4Ω, f = 1kHz, THD + N = 10% | | 17.4 | | W |
| | | $V_{PVDD}$ = 18V, RSPK = 6Ω, f = 1kHz, THD + N = 1% | | 23.5 | | W |
| | | $V_{PVDD}$ = 18V, RSPK = 6Ω, f = 1kHz, THD + N = 10% | | 28.2 | | W |
| | | $V_{PVDD}$ = 21V, RSPK =6Ω, f = 1kHz, THD + N = 1% | | 25.5 | | W |
| | | $V_{PVDD}$ = 24V, RSPK = 8Ω, f = 1kHz, THD + N = 10% | | 32 | | W |
| Total Harmonic Distortion and Noise ($P_O$ = 1W, f = 1kHz, $R_{SPK}$ = 6Ω) | $THD+N_{SPK}$ | $V_{PVDD}$ = 12V, $F_{sw}$ = 768kHz, SPK_GAIN = 13.9Vp/FS, LC-filter, BD mode | | 0.02% | | |
| | | $V_{PVDD}$ = 18V, $F_{sw}$ = 768kHz, SPK_GAIN = 20.8Vp/FS, LC-filter, BD mode | | 0.02% | | |
| Idle Channel Noise (A-Weighted) | $I_{CN(SPK)}$ | $V_{PVDD}$ = 12V, $F_{sw}$ = 768kHz, LC-filter, Load = 6Ω | | 34 | | $μV_{RMS}$ |
| | | $V_{PVDD}$ = 18V, $F_{sw}$ = 768kHz, LC-filter, Load = 6Ω | | 38 | | |
| Dynamic Range | DR | A-Weighted, -60dBFS method. PVDD = 24V, SPK_GAIN = 29.5Vp/FS | | 114 | | dB |
| Power Supply Rejection Ratio | | A-Weighted, referenced to 1% THD + N output level, PVDD = 13.5V | | 108 | | dB |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | $K_{SVR}$ | Injected noise = 1kHz, $1V_{RMS}$, PVDD = 12V, input audio signal = digital zero | | 109 | | dB |
| Crosstalk (Worst Case between Left-to-Right and Right-to-Left Coupling) | $X\text{-}talk_{SPK}$ | f = 1kHz | | 92 | | dB |
| | | | | 102 | | dB |
| AMPLIFIER (MONO PBTL) | | | | | | |
| Total Harmonic Distortion and Noise ($P_O$ = 1W, f = 1kHz) | $THD+N_{SPK}$ | $V_{PVDD}$ = 12V, SPK_GAIN = 16.5Vp/FS, 10μH + 0.68μF filter, $R_{SPK}$ = 4Ω, BD mode | | 0.02% | | |
| | | $V_{PVDD}$ = 24V, SPK_GAIN = 29.5Vp/FS, 10μH + 0.68μF filter, $R_{SPK}$ = 4Ω, 1SPW mode | | 0.04% | | |
| Dynamic Range | DR | A-weighted, –60dBFS method, PVDD = 24V, SPK_GAIN = 29.5Vp/FS | | 114 | | dB |
| Signal-to-Noise Ratio | SNR | A-weighted, referenced to 1% THD + N output level, PVDD = 13.5V | | 108 | | dB |
| | | A-weighted, referenced to 1% THD + N output level, PVDD = 24V | | 109 | | dB |
| Power Supply Rejection Ratio | $K_{SVR}$ | Injected noise = 1kHz, $1V_{RMS}$, PVDD = 19V, input audio signal = digital zero | | 108 | | dB |

## 5.6 TIMING REQUIREMENTS

Table 8 lists the timing.

Table 8. Timing

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| SERIAL AUDIO PORT TIMING | | | | | |
| SCLK Frequency | $f_{SCLK}$ | 1.024 | | | MHz |
| SCLK Period | $t_{SCLK}$ | 40 | | | ns |
| SCLK Pulse Width, Low | $t_{SCLKL}$ | 16 | | | ns |
| SCLK Pulse Width, High | $t_{SCLKH}$ | 16 | | | ns |
| SCLK Rising to LRCK/FS Edge | $t_{SL}$ | 8 | | | ns |
| LRCK/FS Edge to SCLK Rising Edge | $t_{LS}$ | 8 | | | ns |
| Data Setup Time, Before SCLK Rising Edge | $t_{SU}$ | 8 | | | ns |
| Data Hold Time, After SCLK Rising Edge | $t_{DH}$ | 8 | | | ns |
| Data Delay Time from SCLK Falling Edge | $t_{DFS}$ | | | 18 | ns |
| I²C BUS TIMING – STANDARD | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | | | 100 | kHz |
| Bus Free Time Between A STOP and START Condition | $t_{BUF}$ | 4.7 | | | μs |
| Low Period of the SCL Clock | $t_{LOW}$ | 4.7 | | | μs |
| High Period of the SCL Clock | $t_{HI}$ | 4 | | | μs |
| Setup Time for (Repeated) START Condition | $t_{RS-SU}$ | 4.7 | | | μs |
| Hold Time for (Repeated) START Condition | $t_{S-HD}$ | 4 | | | μs |
| Data Setup Time | $t_{D-SU}$ | 250 | | | ns |
| Data Hold Time | $t_{D-HD}$ | 0 | | 3450 | ns |
| Rise Time of SCL Signal | $t_{SCL-R}$ | $20 + 0.1C_B$ | | 1000 | ns |
| Rise Time of SCL Signal After A Repeated START Condition and After An Acknowledge Bit | $t_{SCL-R1}$ | $20 + 0.1C_B$ | | 1000 | ns |
| Fall Time of SCL Signal | $t_{SCL-F}$ | $20 + 0.1C_B$ | | 1000 | ns |
| Rise Time of SDA Signal | $t_{SDA-R}$ | $20 + 0.1C_B$ | | 1000 | ns |
| Fall Time of SDA Signal | $t_{SDA-F}$ | $20 + 0.1C_B$ | | 1000 | ns |
| Setup Time for STOP Condition | $t_{P-SU}$ | 4 | | | μs |
| Capacitive Load for Each Bus Line | $C_B$ | | | 400 | pF |
| I²C BUS TIMING – FAST | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | | | 400 | kHz |
| Bus Free Time Between A STOP and START Condition | $t_{BUF}$ | 1.3 | | | μs |
| Low Period of the SCL Clock | $t_{LOW}$ | 1.3 | | | μs |
| High Period of the SCL Clock | $t_{HI}$ | 600 | | | ns |
| Setup Time for (Repeated) START Condition | $t_{RS-SU}$ | 600 | | | ns |
| Hold Time for (Repeated) START Condition | $t_{RS-HD}$ | 600 | | | ns |
| Data Setup Time | $t_{D-SU}$ | 100 | | | ns |
| Data Hold Time | $t_{D-HD}$ | 0 | | 900 | ns |
| Rise Time of SCL Signal | $t_{SCL-R}$ | $20 + 0.1C_B$ | | 300 | ns |
| Rise Time of SCL Signal After A Repeated START Condition and After An Acknowledge Bit | $t_{SCL-R1}$ | $20 + 0.1C_B$ | | 300 | ns |
| Fall Time of SCL Signal | $t_{SCL-F}$ | $20 + 0.1C_B$ | | 300 | ns |
| Rise Time of SDA Signal | $t_{SDA-R}$ | $20 + 0.1C_B$ | | 300 | ns |
| Fall Time of SDA Signal | $t_{SDA-F}$ | $20 + 0.1C_B$ | | 300 | ns |
| Setup Time for STOP Condition | $t_{P-SU}$ | 600 | | | ns |
| Pulse Width of Spike Suppressed | $t_{SP}$ | | | 50 | ns |
| Capacitive Load for Each Bus Line | $C_B$ | | | 400 | pF |

# 5.7 TYPICAL CHARACTERISTICS

## 5.7.1 BRIDGE TIED LOAD (BTL) CONFIGURATION CURVES WITH 1SPW MODE

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using AU6825 EVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements were taken with audio frequency set to 1kHz and device PWM Modulation mode set to 1SPW mode with Class D Bandwidth = 120kHz for 576kHz $F_{sw}$ and Class D Bandwidth = 175kHz for 768kHz $F_{sw}$ (liste in register 0x53) unless otherwise noted.

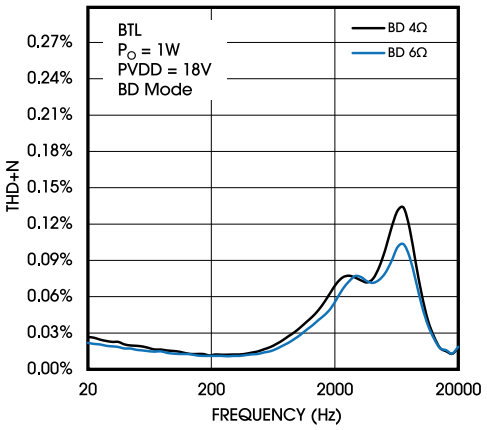



Figure 2. THD + N vs. Frequency-BTL, 10uH, 768KHz

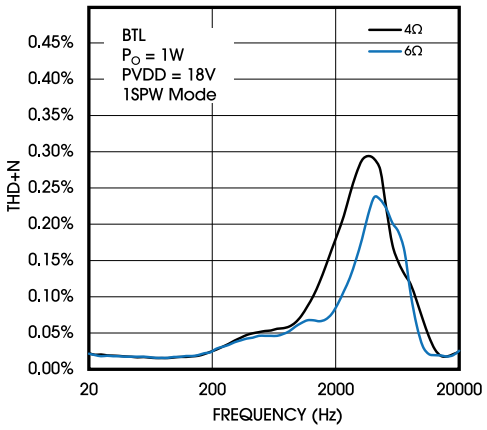



Figure 3. THD + N vs. Frequency-BTL

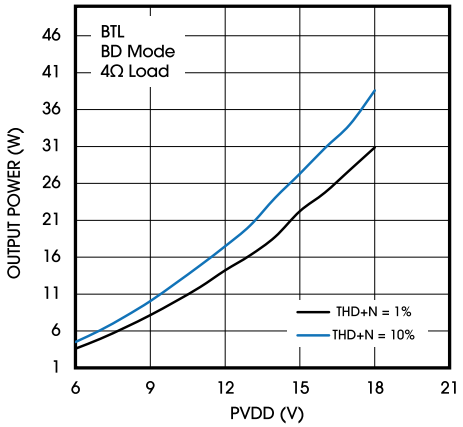



Figure 4. Output Power vs. Supply Voltage (BTL)

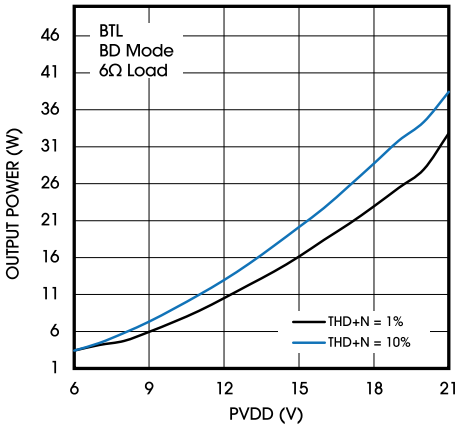



Figure 5. Output Power vs. Supply Voltage (BTL)

# 6. PARAMETER MEASUREMENT INFORMATION

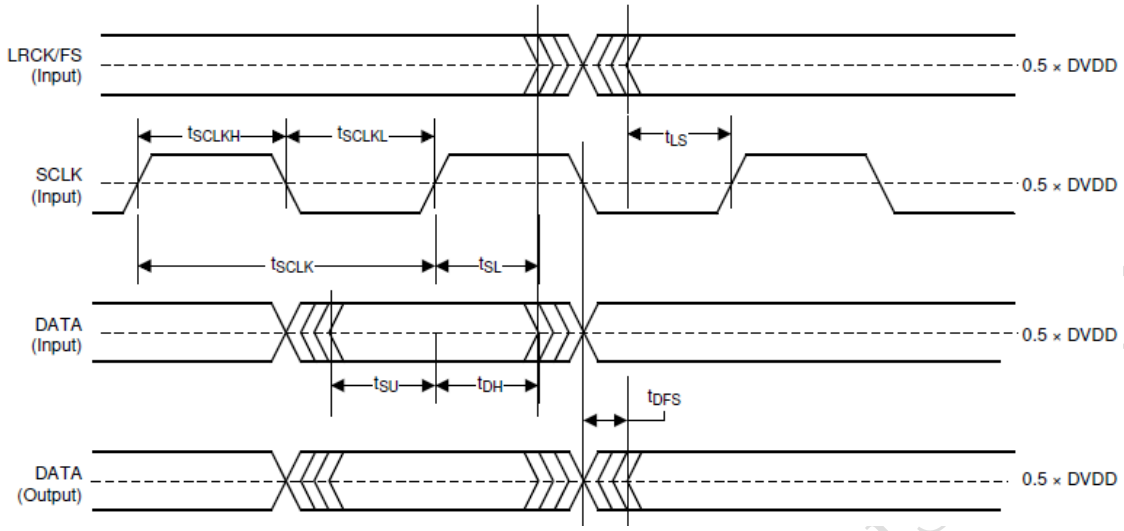



Figure 6. Serial Audio Port Timing in Slave Mode

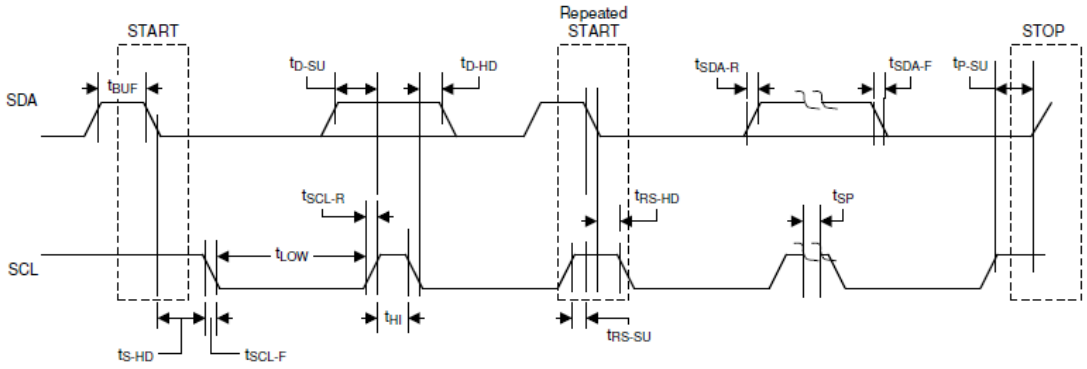



Figure 7. I²C Communication Port Timing Diagram



# 7. 详细描述

## 7.1 概述

AU6825 主要由 5 个部分组成，包括：

- 一个立体声 DACA
- 32bit 高精度音频 DSP
- 闭环架构的 Class D
- I2C 控制接口
- 保护逻辑和内部 ADC 电压温度采样模块

PVDD 供电电压范围为 4.5V 到 26.4V, DVDD 支持 3.3V 或者 1.8V 逻辑。此外 AU6825 提供两个 GPIO，可以配置成回声消除或者其他 GPIO 功能，例如 fault。此外 AU6825 支持 32k-192k 输入采样率。

## 7.2 功能模块框图

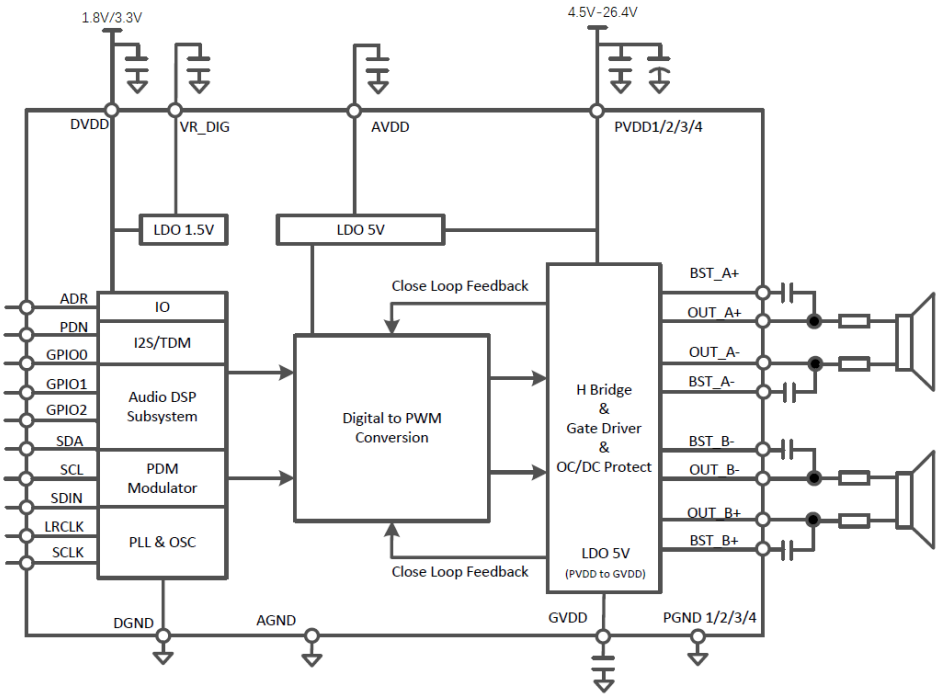



Figure 8. Functional Block Diagram

# 7.3 特性说明

## 7.3.1 串行音频接口及频率

AU6825 支持的音频输入数据格式和频率配置如下表所示：

Table 9. Audio Data Formats, Bit Depths, and Clock Rates

| FORMAT | DATA BITS | MAXIMUM LRCLK/FS FREQUENCY (kHz) | SCLK RATE ($f_S$) |
|---|---|---|---|
| I²S/LJ/RJ | 32, 24, 20, 16 | 32 to 192 | 64, 32 |
| TDM | 32, 24, 20, 16 | 32 | 128 |
| | | 44.1, 48 | 128, 256, 512 |
| | | 96 | 128, 256 |
| | | 192 | 128 |

## 7.3.2 时钟停止及恢复

AU6825 支持时钟频率停止后自动进入 Hiz 或者其他低功耗模式，时钟恢复后可以自动恢复。

## 7.3.3 在线改变采样率

AU6825 支持在线编辑 EQ 等参数，此外还支持自动切换采样率功能。通常情况为了避免 pop 音，建议进入 Hiz 或者 sleep 等状态后再进行采样率切换。

## 7.3.4 串行音频接口-数据格式和有效位

AU6825 支持如下 I2S 格式：

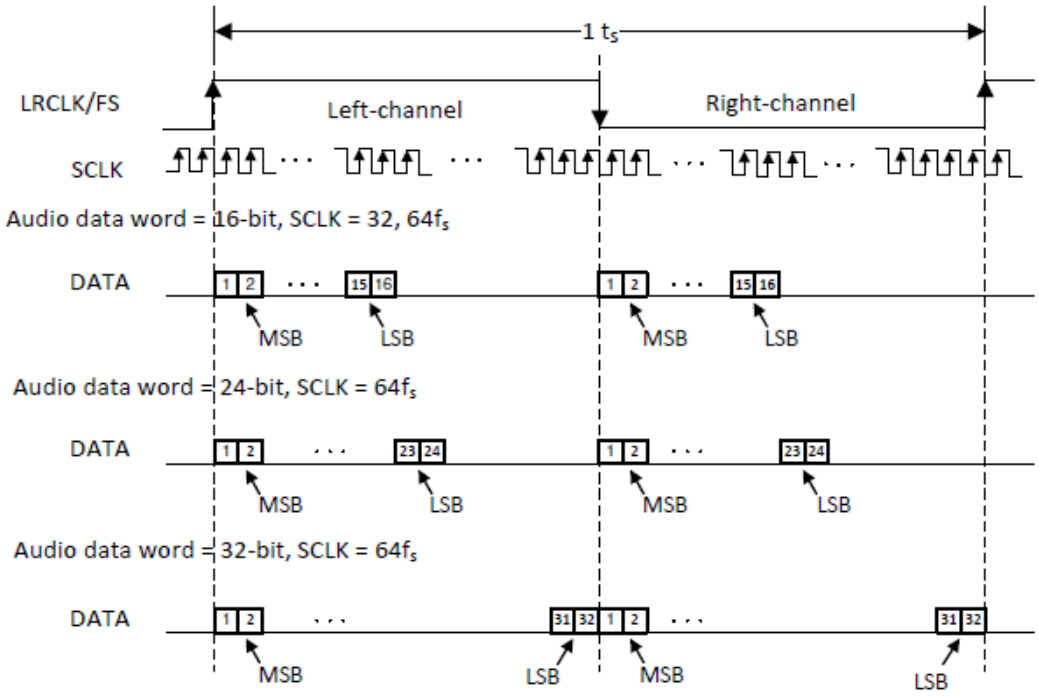
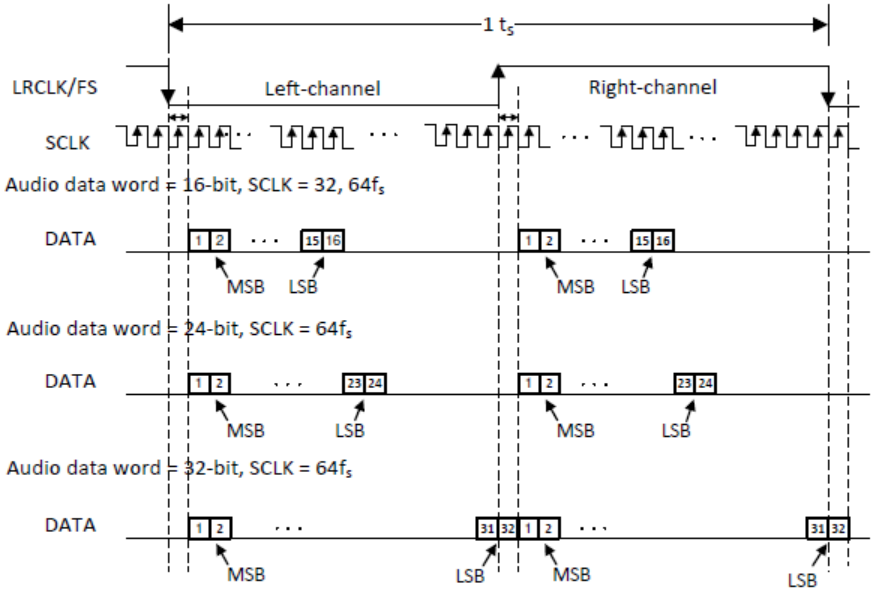
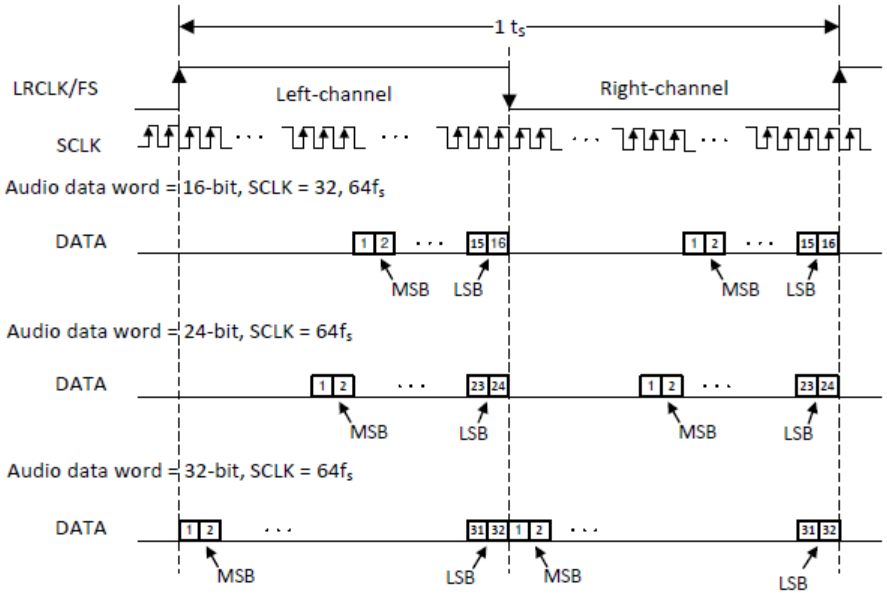



Figure 9. Left-Justified Audio Data Format




$I^2S$ Data Format; L-channel = LOW, R-channel = HIGH

Figure 10. $I^2S$ Audio Data Format




Right-Justified Data Format; L-channel = HIGH, R-channel = LOW

Figure 11. Right-Justified Audio Data Format

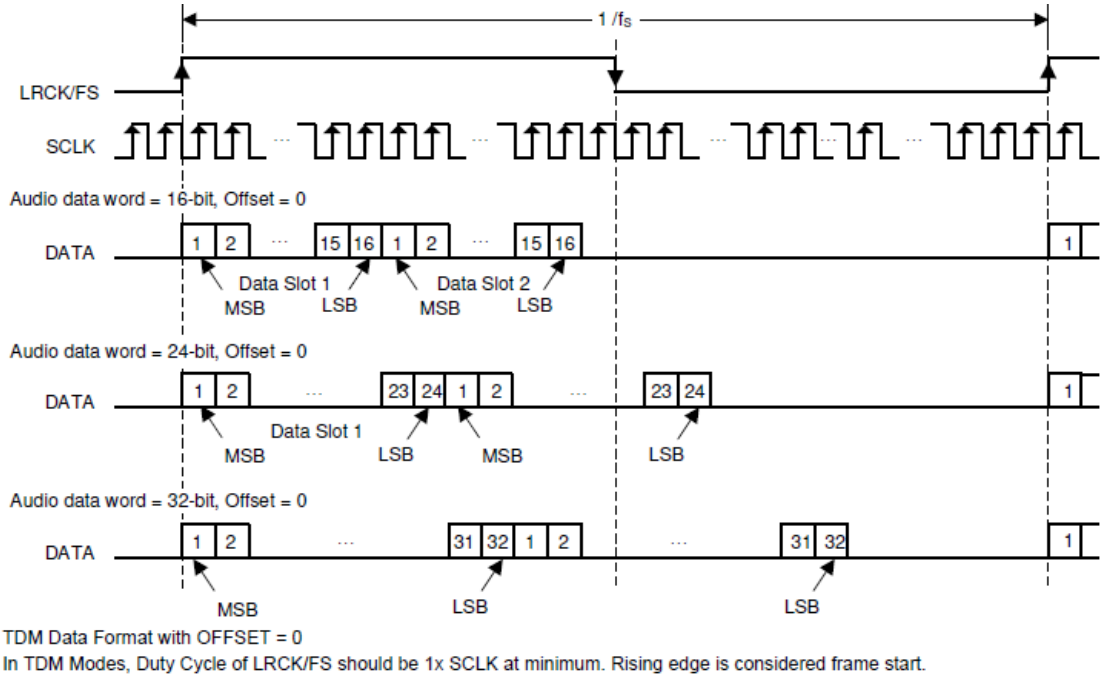



Figure 12. TDM 1 Audio Data Format

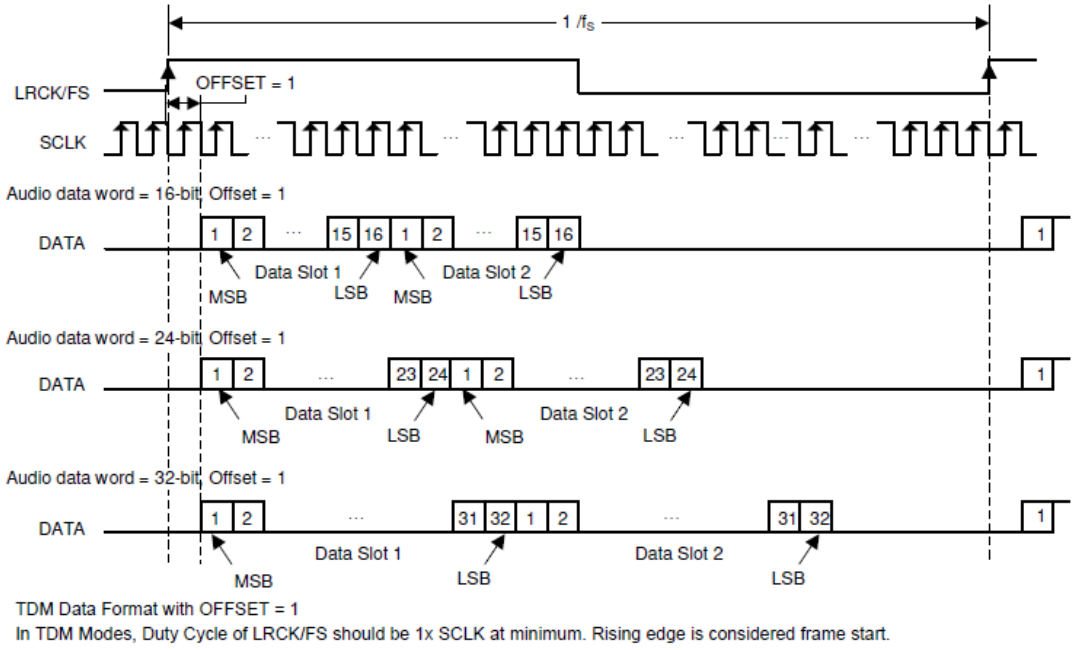



Figure 13. TDM 2 Audio Data Format

## 7.3.5 数字音频处理

AU6825 DSP 支持多种音频处理的算法结构，配置上包括立体声 2.0， 高低音 1.1 或者 2.1 或者 2.2 模式。

1. 简单模式：SRC + 2*15*EQ + 1-band DRC + AGL
2. 标准模式：SRC + 2*15 EQs + 3-band DRC + AGL + 3 post-EQ
3. 高阶模式：SRC + 2*15 Eqs + DPEQ + 3-band DRC + AGL + 3 Post-EQ
4. Class H 算法

类比半导体提供一站式调音平台，该平台可以直接产生配置脚本。

## 7.3.6 功放增益选择

如下图，基本结果如下图所示：

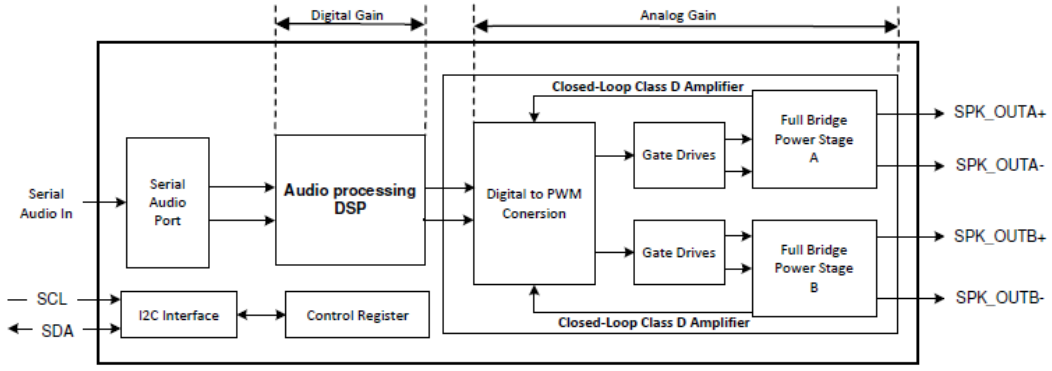



Figure 14. Speaker Amplifier Gain

配置增益主要通过模拟的增益，即寄存器 0x54, Book 0, page0。其对应的输出 peak 值如下表所示。此外 DSP 部分也可以配置增益，但是该增益收到 AGL DRC 的门限限制。

Table 10. Analog Gain Setting

| AGAIN(4: 0) | GAIN (dBFS) | IPLIFIER PEAKOUTPUT VOLTAGE (V) |
|---|---|---|
| 00000 | 0 | 29.5 |
| 00001 | -0.5 | 27.85 |
| ……. | …….. | ……. |
| 11111 | -15.5 | 4.95 |

# 7.4 DEVICE FUNCTIONAL MODES

## 7.4.1 SOFTWARE CONTROL

The AU6825 device is configured via an I²C communication port.

TheI²C Communication Protocol is detailed in the I²C COMMUNICATION PORT section. The I²C timing requirements are described in the I²C BUS TIMING – STANDARD and I²C BUS TIMING – FAST sections.

## 7.4.2 SPEAKER AMPLIFIEROPERATING MODES

The AU6825 device can be used in two different amplifier configurations:

- BTL mode
- PBTL mode

### 7.4.2.1 BTL MODE

In BTL mode, the AU6825 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A + and OUT_A–, the amplified right signal is presented on differential output pair shown as OUT_B + and OUT_B–.

### 7.4.2.2 PBTL MODE

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the AU6825 device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows for smaller, less-expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the AU6825 device, the input signal to the PBTL amplifier is left frame of I²S or TDM data.

## 7.4.3 芯片状态控制

AU6825 主要有 5 种模式：

- Shutdown mode：$\overline{\text{PDN}}$ 拉低后内部 LDO 都会关闭，此时功耗最低。

- Deep Sleep mode：深度睡眠模式下，I2C 通讯可以正常，数字核的供电也正常，模拟部分 LDO 关闭， DSP 处于活动状态。
- Sleep mode. 该模式下，I2C 模块，数字核，DSP 和 deep sleep 模式一样正常工作，此外模拟部分 5V Analog LDO 会正常工作。
- Output Hi-Z mode：除了输出 power stage 外，都处于 active 状态。
- Play mode. When register 0x03h-D(1:0) = 11, device stays in Play mode.

## 7.4.4 芯片调制模式

### 7.4.4.1 BD 工作模式：

AU6825 支持 BD 模式，单边工作模式。

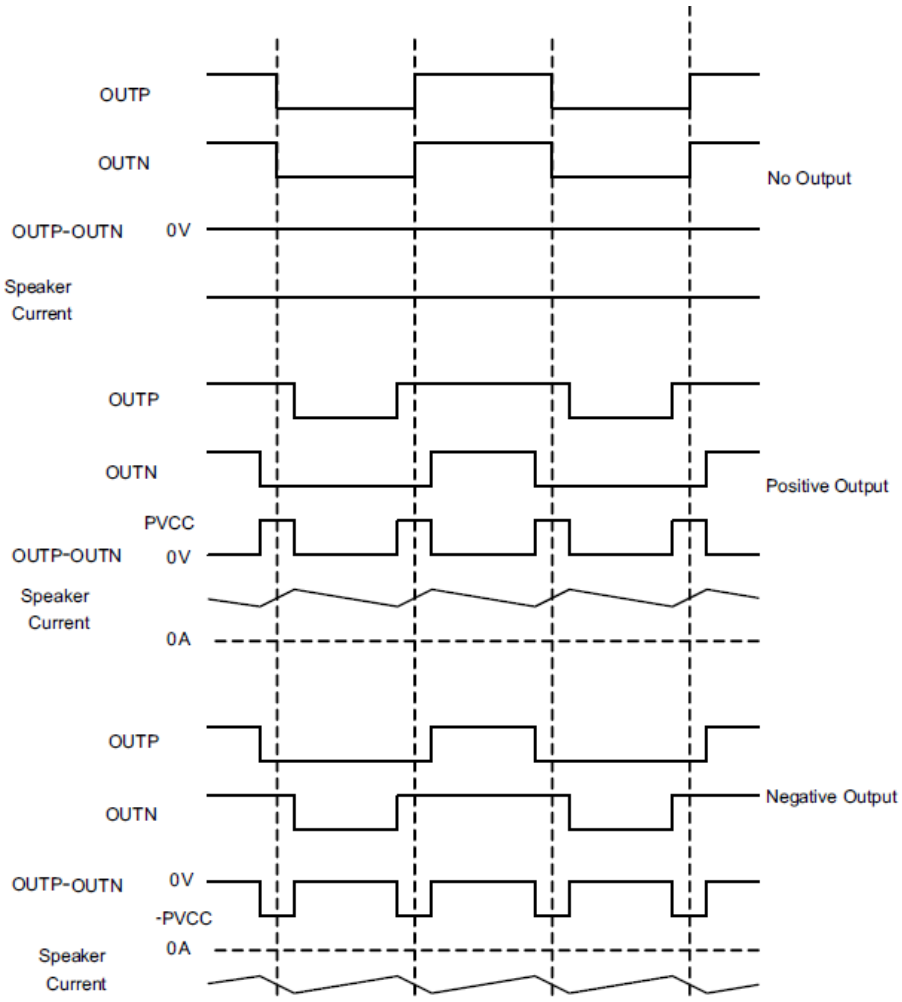



Figure 15. BD Mode Modulation

### 7.4.4.2 1SPW MODULATION

单边工作模式：

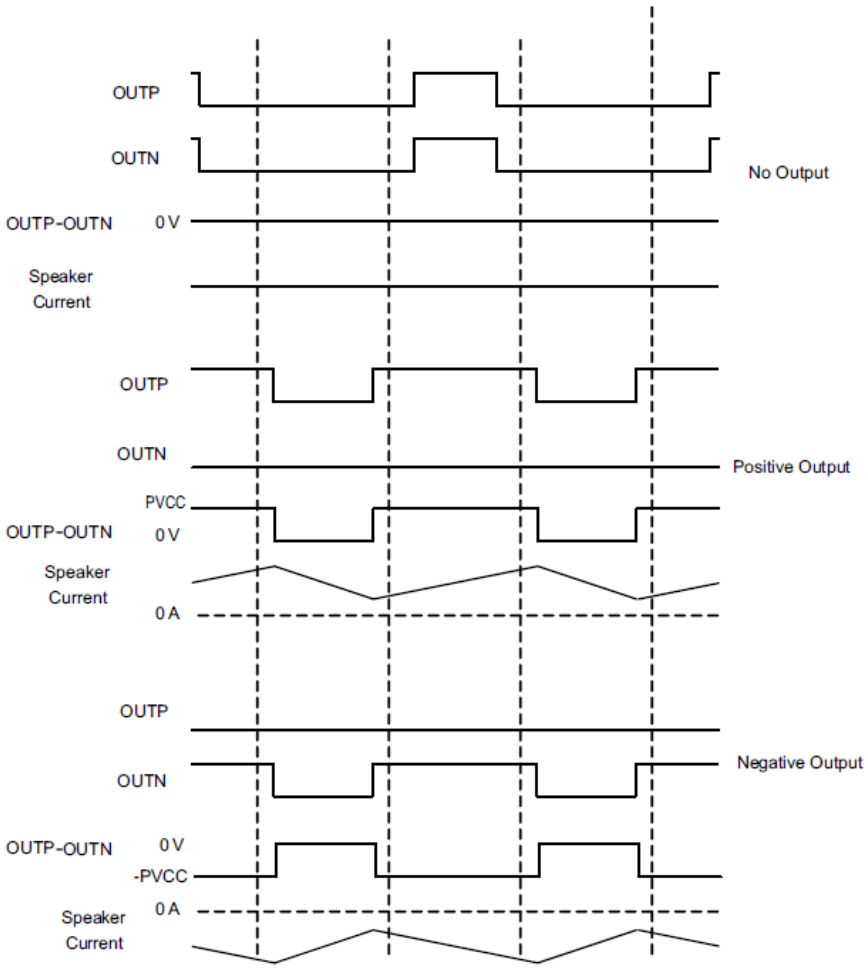



Figure 16. 1SPW Mode Modulation

# 7.5 编程和控制

## 7.5.1 I²C SERIAL COMMUNICATION BUS

AU6825 支持标准或者 fast I2C，标称寻址方式分为 book， page 和 register 的架构。

# 7.6 从机地址

从机地址通过 ADR 管脚进行配置，具体包括：

Table 11. I²C Slave Address Configuration

| ADR PIN CONFIGURATION | MSB | | | | | USER-DEFINED | | LSB |
|---|---|---|---|---|---|---|---|---|
| 0kΩ to DGND | 1 | 0 | 0 | 1 | 1 | 0 | 0 | R/$\overline{W}$ |
| 1kΩ to DGND | 1 | 0 | 0 | 1 | 1 | 0 | 1 | R/$\overline{W}$ |
| 4.7kΩ to DGND | 1 | 0 | 0 | 1 | 1 | 1 | 0 | R/$\overline{W}$ |
| 15kΩ to DGND | 1 | 0 | 0 | 1 | 1 | 1 | 1 | R/$\overline{W}$ |
| 33kΩ to DVDD | 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |
| 6.8kΩ to DVDD | 1 | 0 | 1 | 0 | 0 | 0 | 1 | R/$\overline{W}$ |
| 0kΩ to DVDD | 硬件控制模式 | | | | | | | |

### 7.6.1.1 随机写入

随机写入格式如下：

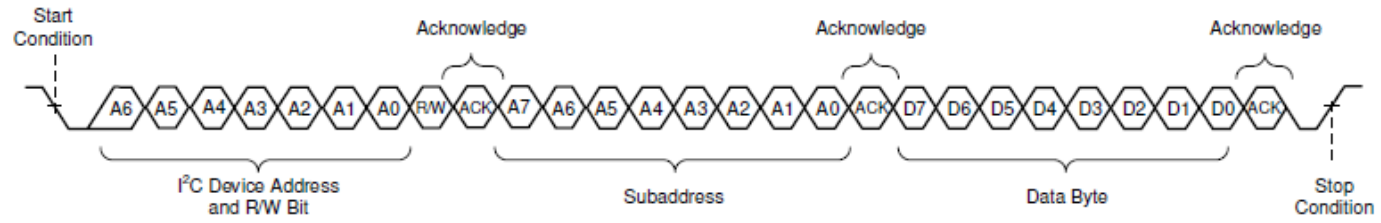



Figure 17. Random Write Transfer

### 7.6.1.2 顺序写入

顺序写入格式如下：

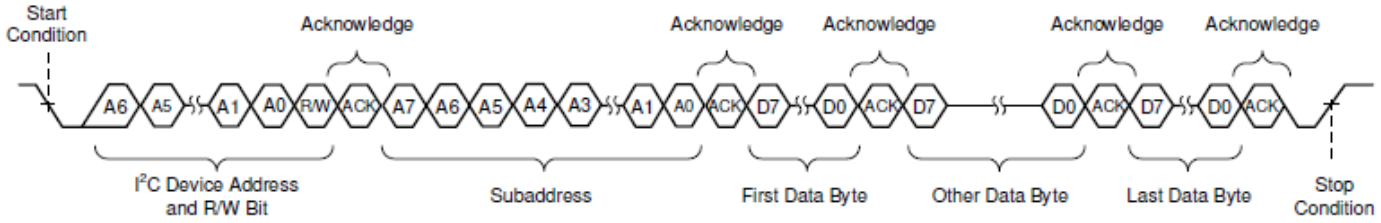



Figure 18. Sequential Write Transfer

### 7.6.1.3 随机读取

随机读取如下：

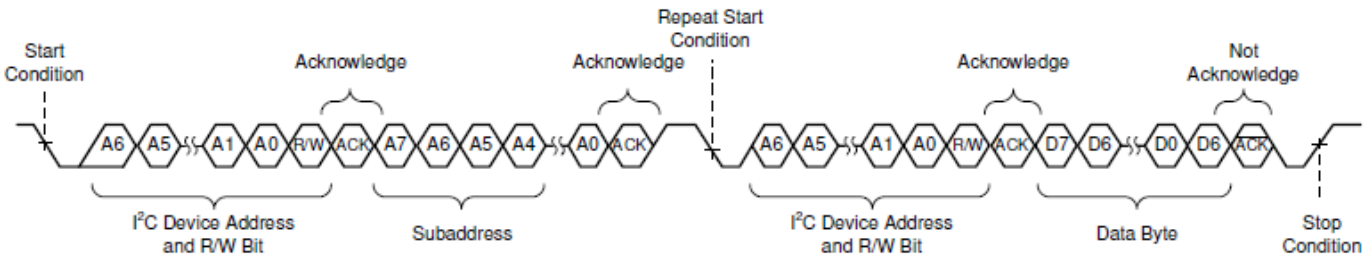



Figure 19. Random Read Transfer

### 7.6.1.4 顺序读取

顺序读取时序如下：

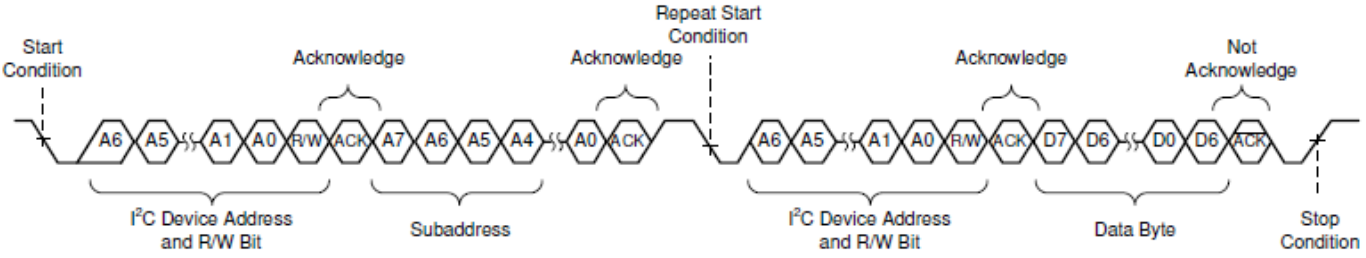



Figure 20. Sequential Read Transfer

### 7.6.1.5 内存空间结构及参数更新

AU6825 book 操作通过 0x7f 进入相应的 book, 0x00 进入相应的 page，每次切换 book,需要先进入 page0。每次新进入一个 book，默认就处于 page0.

## 7.6.2 软件控制

### 7.6.2.1 上电时序

1. 配置 ADR/$\overline{\text{FAULT}}$设置 I²C 地址.
2. 建议先 DVDD 再上 PVDD,时间提前量 1ms 即可；
3. 拉高 PDN
4. I2C 进入 play 之前的所有配置，并且中间无需等待时间，且不需要 I2S 时钟存在。
5. 进入 play 之前提供 I2S。然后进入 play 模式即可

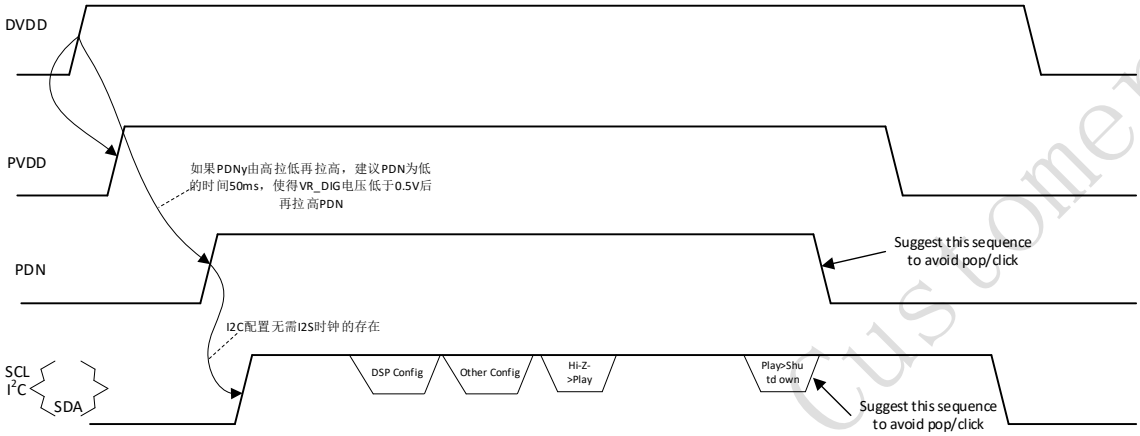



Figure 21. Start-up and Power-down Sequence

### 7.6.2.2 下电时序

1. 芯片正常工作.
2. 配置寄存器使得芯片进入 Hiz 或以下的状态，然后拉低 PDN.
3. 等待 10ms
4. 拉低 PVDD,然后拉低 DVDD;
5. 芯片处于下电状态

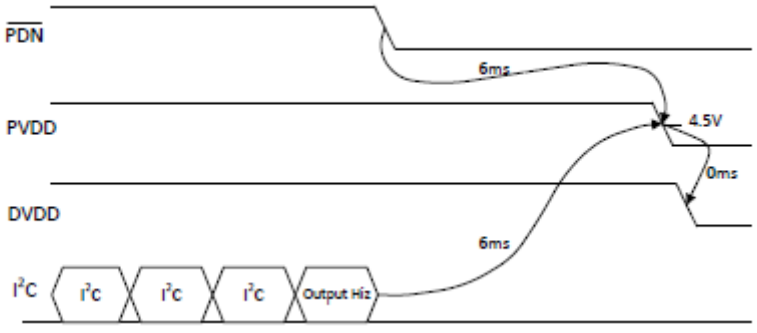



Figure 22. Power-Down Sequence

Before PVDD/DVDD powers down, Class D Output driver needs to be disabled by $\overline{\text{PDN}}$ or by I²C.

At least 6ms delay is needed based on LRCLK (Fs) = 48kHz. Digital volume ramp-down updates every sample period, and decreases by 0.5dB for each update. Digital volume = 24dB. The delay changes when the value of register 0x4C and 0x4E or the LRCLK rate changes.



### 7.6.2.3 保护和监测

#### 7.6.2.3.1 OVERCURRENT SHUTDOWN (OCSD)

在输出发生异常，触发过流保护是，AU6825 可以在 100ns 内关闭功放输,并且通过寄存器上报过流保护出错。AU6825 可以区分判断出哪一个通道发生了过流保护。过流保护是锁存的，在过流异常事件接触后，需要进行错误清除，功放才能够继续正常工作。

#### 7.6.2.3.2 SPEAKER DC PROTECTION

If the device measures a > 1.9V (Typical) DC offset and continues more than 600ms (typical) on the output stage, the ADR/$\overline{\text{FAULT}}$ line will be pulled low and set the OUTxx outputs to Hi-Z state to protect speaker, signifying a fault in register 0x70 in Book0/Page0. This fault report bit in register 0x70 keeps 1 and device keeps in Hi-Z mode unless it is cleared by register 0x78 in Book0/Page0 manually.

#### 7.6.2.3.3 DEVICE OVER TEMPERATURE PROTECTION

Once the die temperature exceeds 160°C (Typical), device will set the output driver from Play mode to Hi-Z mode. Over temperature shutdown fault is reported by register 0x72 in Book0/Page0. Set this fault's behavior to Auto-Recovery mode, device will come back to Play mode automatically once the die temperature drops down to 150°C or device needs re-enter into Play mode by clearing fault with register 0x78 in Book0/Page0.

#### 7.6.2.3.4 DEVICE OVER VOLTAGE/UNDER VOLTAGE PROTECTION

##### 7.6.2.3.4.1 OVER VOLTAGE PROTECTION

Once the PVDD voltage exceeds the $OVE_{THRES\ (PVDD)}$ (28.1V Typical), device will set the output driver from Play mode to Hi-Z mode, and over voltage fault is reported by register 0x71 in Book0/Page0. Once PVDD drops below 27.5V (Typical), device will come back to Play mode. But this bit still keeps 1 unless cleared by register 0x78 in Book0/Page0 manually.

##### 7.6.2.3.4.2 UNDER VOLTAGE PROTECTION

Once the PVDD voltage drops below the $UVE_{THRES\ (PVDD)}$ (4V Typical), device will set the output driver from Play mode to Hi-Z mode, and under voltage fault is reported by register 0x71 in Book0/Page0. Once PVDD rises above 4.26.4V (Typical), device will come back to Play mode. But this bit still keeps 1 unless cleared by register

0x0D in Book0/Page0 manually.

#### 7.6.2.3.5 CLOCK FAULT

如果发生 Clock Halt, SCLK/LRCLK Ratio Error, PLL unlock, FS error, register 0x37 和 register 0x39 会实时监测，此时芯片可以通过寄存器配置进入 hiz 或者 sleep 模式，从而实现低功耗。Clock fault 可以在寄存器 0x71 中读取。

# 8. REGISTER MAP

## 8.1.1 CONTROL PORT REGISTERS

Table 14 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in Table 14 should be considered as reserved locations and the register contents should not be modified.

Table 12. CONTROL PORT Registers

| OFFSET | ACRONYM | REGISTER NAME |
|---|---|---|
| 1h | RESET_CTRL | Register 1 |
| 2h | DEVICE_CTRL_1 | Register 2 |
| 3h | DEVICE_CTRL_2 | Register 3 |
| Dh | RESET_CTRL_2 | Register 13 |
| Fh | I2C_PAGE_AUTO_INC | Register 15 |
| 28h | SIG_CH_CTRL | Register 40 |
| 29h | CLOCK_DET_CTRL | Register 41 |
| 30h | SDOUT_SEL | Register 48 |
| 31h | I2S_CTRL | Register 49 |
| 33h | SAP_CTRL1 | Register 51 |
| 34h | SAP_CTRL2 | Register 52 |
| 35h | SAP_CTRL3 | Register 53 |
| 37h | FS_MON | Register 55 |
| 38h | BCK_MON | Register 56 |
| 39h | CLKDET_STATUS | Register 57 |
| 4Ch | DIG_VOL_CTRL | Register 76 |
| 4Eh | DIG_VOL_CTRL2 | Register 78 |
| 4Fh | DIG_VOL_CTRL3 | Register 79 |
| 53h | ANA_CTRL | Register 83 |
| 54h | AGAIN | Register 84 |
| 5Ch | BQ_WR_CTRL1 | Register 92 |
| 62h | GPIO0 | Register 98 |
| 63h | GPIO1 | Register 99 |
| 64h | GPIO2 | Register 100 |
| 67h | Die ID | Register 105 |
| 6Ah | PHASE_CTRL | Register 108 |
| 6Bh | SS_CTRL0 | Register 107 |
| 6Ch | SS_CTRL1 | Register 108 |
| 6Dh | SS_CTRL2 | Register 109 |
| 6Eh | SS_CTRL3 | Register 110 |
| 6Fh | SS_CTRL4 | Register 111 |
| 70h | CHAN_FAULT | Register 112 |
| 71h | GLOBAL_FAULT1 | Register 113 |
| 72h | GLOBAL_FAULT2 | Register 114 |
| 73h | OT WARNING | Register 115 |
| 74h | PIN_CONTROL1 | Register 116 |
| 75h | PIN_CONTROL2 | Register 117 |
| 76h | MISC_CONTROL | Register 118 |

Complex bit access types are encoded to fit into small table cells. Table 15 shows the codes that are used for access types in this section.

Table 13. CONTROL PORT Access Type Codes

| ACCESS TYPE | CODE | DESCRIPTION |
|---|---|---|



| READ TYPE | | |
|---|---|---|
| R | R | Read |
| WRITE TYPE | | |
| W | W | Write |
| RESETOR DEFAULT VALUE | | |
| -n | | Value after reset or the default value |

### 8.1.1.1 RESET_CTRL REGISTER (OFFSET = 1H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 14. RESET_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | RST_MOD | RESERVED | | | RST_REG |
| R/W | | | W | R | | | W |

Table 15. RESET_CTRL Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:5 | RESERVED | R/W | 000 | Reserved |
| 4 | RST_MOD | W | 0 | WRITE CLEAR BIT<br>Reset Modules<br>This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in hiz mode.<br>0: Normal<br>1: Reset modules |
| 3:1 | RESERVED | R | 000 | Reserved |
| 0 | RST_REG | W | 0 | Write clear bit<br>Reset Registers<br>This bit resets the mode registers back to their initial values. The RAM content is not cleared. This bit is auto cleared and must be set only when the DAC is in hiz mode (resetting registers when the DAC is running is prohibited and not supported).<br>0: Normal<br>1: Reset mode registers” |

### 8.1.1.2 DEVICE_CTRL_1 REGISTER (OFFSET = 2H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 16. DEVICE_CTRL_1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | FSW_SEL | | | RESERVED | MP_PBTL | DAMP_MOD | |
| R/W | R/W | | | R/W | R/W | R/W | |

Table 17. DEVICE_CTRL_1 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | Reserved | R/W | 0 | Reserved |
| 6:4 | FSW_SEL | R/W | 000 | select fsw (kHz):<br>0: 260<br>1: 310<br>2: 384<br>3: 480<br>4: 576<br>5: 768<br>others：reserved |
| 3 | RESERVED | R/W | 0 | Reserved |
| 2 | DAMP_PBTL | R/W | 0 | 0: Set DAMP to BTL mode<br>1: Set DAMP to PBTL mode |
| 1:0 | DAMP_MOD | R/W | 00 | 00: BD mode<br>01: 1SPW mode<br>10: Hybrid mode |

### 8.1.1.3 DEVICE_CTRL_2 REGISTER (OFFSET = 3H) [RESET = 0X10]

Return to SUMMARY TABLE.

Table 18. DEVICE_CTRL_2 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | DEEPSLEEP_ON_CLKF | MANUAL_MODE | DIS_DSP | MUTE | RESERVED | CTRL_STATE | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

Table 19. DEVICE_CTRL_2 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | RESERVED | R/W | | Reserved |
| 6 | DEEPSLEEP_ON_CLKF | R/W | 0 | Power state goes to DEEPSLEEP when I2S clock fault happens |
| 5 | MANUAL_MODE | R/W | 0 | Device in manual mode,<br>Sample_rate is configured by reg_fs_cfg and all the divider ratios need to be configured. |
| 4 | DIS_DSP | R/W | 1 | DSP reset<br>When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync.<br>0: Normal operation<br>1: Reset the DSP |
| 3 | MUTE | R/W | 0 | Mute left/right channel<br>This bit issues soft mute request for the left/right channel. The volume will be smoothly ramped down/up to avoid pop/click noise.<br>0: Normal volume<br>1: Mute |
| 2 | RESERVED | R/W | 0 | Reserved |
| 1:0 | CTRL_STATE | R/W | 00 | Device state control register<br>00: Deep Sleep<br>01: Sleep<br>10: Hi-Z<br>11: Play |

### 8.1.1.4 RESET_CTRL_2 REGISTER (OFFSET = DH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 20. DEVICE_CTRL_2 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Sync_done | RESERVED | | | | | CTRL_STATE | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

Table 21. DEVICE_CTRL_2 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | RESERVED | R/W | | 1: sync is properly done |
| 6:1 | RESERVED | R/W | 0 | Reserved. |
| 0 | Clear Fault | R/W | 0 | 1: clear analog fault |

### 8.1.1.5 I2C_PAGE_AUTO_INC REGISTER (OFFSET = FH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 22. I2C_PAGE_AUTO_INC Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | PAGE_AUTOINC_DIS | RESERVED | | |
| R/W | | | | R/W | R/W | | |

Table 23. I2C_PAGE_AUTO_INC Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:4 | RESERVED | R/W | 0000 | Reserved |
| 3 | PAGE_AUTOINC_DIS | R/W | 0 | Page auto increment disable<br>Disable page auto increment mode for non-zero books. When end of page is reached, it goes back to the 8th address location of next page when this bit is 0. When this bit is 1, it goes to the 0th location of current page itself like in older part.<br>0: Enable Page auto increment<br>1: Disable Page auto increment |
| 2:0 | RESERVED | R/W | 000 | Reserved |

#### 8.1.1.6 SIG_CH_CTRL REGISTER (OFFSET = 28H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 24. SIG_CH_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BCK_RATIO_CONFIGURE | | | | FS_CFG | | | |
| R/W | | | | R/W | | | |

Table 25. SIG_CH_CTRL Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:4 | BCK_RATIO_CONFIGURE | R/W | 0000 | These bits indicate the configured BCK ratio, the number of BCK clocks in one audio frame.<br>0011: 32FS<br>0101: 64FS<br>0111: 128FS<br>1001: 256FS<br>1011: 512FS |
| 3:0 | FS_CFG | R/W | 0000 | FS Speed Mode<br>These bits select the FS operation mode, which must be set according to the current audio sampling rate.<br>4'b0000 Auto detection<br>4'b0110 32KHz<br>4'b1000 44.1KHz<br>4'b1001 48KHz<br>4'b1010 88.2KHz<br>4'b1011 96KHz<br>4'b1101 192KHz<br>Others Reserved |

### 8.1.1.7 CLOCK_DET_CTRL REGISTER (OFFSET = 29H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 26. CLOCK_DET_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | DIS_DET_PLL | DIS_DET_BCLK_RANGE | DIS_DET_FS | DIS_DIS_DET_BCLK | DIS_DET_MISS | RESERVED | RESERVED |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 27. CLOCK_DET_CTRL Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 0 | Reserved |
| 6 | DIS_DET_PLL | R/W | 0 | Ignore PLL underrate/overate Detection<br>This bit controls whether to ignore the PLL underrate/overrate detection. The PLL clock must be faster than 10MHz or an error will be reported. The PLL must be slower than 150MHz or an error will be reported. When ignored, a PLL underrate/overrate error will not cause a clock error.<br>0: Regard PLL underrate/overrate detection<br>1: Ignore PLL underrate/overrate detection |
| 5 | DIS_DET_BCLK_RANGE | R/W | 0 | Ignore BCK Range Detection<br>This bit controls whether to ignore the BCK range detection. The BCK must be stable between 256KHz and 50MHz or an error will be reported. When ignored, a BCK range error will not cause a clock error.<br>0: Regard BCK Range detection<br>1: Ignore BCK Range detection |
| 4 | DIS_DET_FS | R/W | 0 | Ignore FS Error Detection<br>This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error. But CLKDET_STATUS will report fs error.<br>0: Regard FS detection<br>1: Ignore FS detection |
| 3 | DIS_DET_BCLK | R/W | 0 | Ignore BCK Detection<br>This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error.<br>0: Regard BCK detection<br>1: Ignore BCK detection |
| 2 | DIS_DET_MISS | R/W | 0 | Ignore BCK Missing Detection<br>This bit controls whether to ignore the BCK missing detection. When ignored an BCK missing will not cause a clock error.<br>0: Regard BCK missing detection<br>1: Ignore BCK missing detection |
| 1 | RESERVED | R/W | 0 | Reserved |
| 0 | RESERVED | R/W | 0 | Reserved |

### 8.1.1.8 SDOUT_SEL REGISTER (OFFSET = 30H) [RESET = 0H]

Return to SUMMARY TABLE.

Table 28. SDOUT_SEL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | SDOUT_SEL |
| | | | | | | | R/W |

Table 29. SDOUT_SEL Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:1 | RESERVED | | 0 | Reserved |
| 0 | SDOUT_SEL | RW | 0 | SDOUT Select.<br>This bit selects what is being output as SDOUT pin.<br>0: SDOUT is the DSP output (post-processing)<br>1: SDOUT is the DSP input (pre-processing) |

### 8.1.1.9 I2S_CTRL REGISTER (OFFSET = 31H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 30. I2S_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | BCK_INV | RESERVED | | RESERVED | | RESERVED |
| R/W | | R/W | R/W | R | R | | R/W |

Table 31. I2S_CTRL Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | RESERVED | R/W | 00 | Reserved |
| 5 | BCK_INV | R/W | 0 | BCK Polarity<br>This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK.<br>0: Normal BCK mode<br>1: Inverted BCK mode |
| 4:0 | RESERVED | R/W | 00000 | Reserved |

### 8.1.1.10 SAP_CTRL1 REGISTER (OFFSET = 33H) [RESET = 0X02]

Return to SUMMARY TABLE.

Table 32. SAP_CTRL1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| I2S_SHIFT_MSB | RESERVED | DATA_FORMAT | | I2S_LRCLK_PULSE | | WORD_LENGTH | |
| R/W | R/W | R/W | | R/W | | R/W | |

Table 33. SAP_CTRL1 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | I2S_SHIFT_MSB | R/W | 0 | I²S shift MSB |
| 6 | RESERVED | R/W | 0 | Reserved |
| 5:4 | DATA_FORMAT | R/W | 00 | I²S data format<br>These bits control both input and output audio interface formats for DAC operation.<br>00: I²S<br>01: TDM/DSP<br>10: RTJ<br>11: LTJ |
| 3:2 | I2S_LRCLK_PULSE | R/W | 00 | 01: LRCLK pulse < 8 SCLK. If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, these two bits need set to 01. |
| 1:0 | WORD_LENGTH | R/W | 10 | I²S word length<br>These bits control both input and output audio interface sample word lengths for DAC operation.<br>00: 16 bits<br>01: 20 bits<br>10: 24 bits<br>11: 32 bits |

### 8.1.1.11 SAP_CTRL2 REGISTER (OFFSET = 34H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 34. SAP_CTRL2 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| I2S_SHIFT_LSB | | | | | | | |
| R/W | | | | | | | |

Table 35. SAP_CTRL2 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:0 | I2S_SHIFT | R/W | 00000000 | I²S shift LSB<br>I2S Shift LSB<br>These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample.<br>000000000: offset = 0 BCK (no offset)<br>000000001: offset = 1 BCK<br>000000010: offset = 2 BCKs<br>…<br>111111111: offset = 512 BCKs |



### 8.1.1.12 SAP_CTRL3 REGISTER (OFFSET = 35H) [RESET = 0X11]

Return to SUMMARY TABLE.

Table 36. SAP_CTRL3 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | LEFT_DAC_DPATH | | RESERVED | | RIGHT_DAC_DPATH | |
| R/W | | R/W | | R/W | | R/W | |

Table 37. SAP_CTRL3 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | RESERVED | R/W | 00 | Reserved |
| 5:4 | LEFT_DAC_DPATH | R/W | 01 | Left DAC Data Path<br>These bits control the left channel audio data path connection.<br>00: Zero data (mute)<br>01: Left channel data<br>10: Right channel data<br>11: Reserved (do not set) |
| 3:2 | RESERVED | R/W | 00 | Reserved |
| 1:0 | RIGHT_DAC_DPATH | R/W | 01 | Right DAC Data Path<br>These bits control the right channel audio data path connection.<br>00: Zero data (mute)<br>01: Right channel data<br>10: Left channel data<br>11: Reserved (do not set) |

### 8.1.1.13 FS_MON REGISTER (OFFSET = 37H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 38. FS_MON Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | BCLK_RATIO_MSB | | FS_RPT | | | |
| R/W | | R | | R | | | |

Table 39. FS_MON Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | RESERVED | R/W | 00 | Reserved |
| 5:4 | BCLK_RATIO_HIGH | R | 00 | 2 MSBs of detected BCK ratio |
| 3:0 | FS_RPT | R | 0000 | These bits indicate the currently detected audio sampling rate.<br>4'b0000 FS Error<br>4'b0110 32KHz<br>4'b1000 Reserved<br>4'b1001 48KHz<br>4'b1011 96KHz<br>4'b1100 176.4KHz<br>4'b1101 192KHz<br>Others Reserved |

### 8.1.1.14 BCK_MON REGISTER (OFFSET = 38H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 40. BCK_MON Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BCLK_RATIO_LSB | | | | | | | |
| R | | | | | | | |

Table 41. BCK_MON Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | BCLK_RATIO_LSB | R | 00000000 | These bits indicate the currently detected BCK ratio, the number of BCK clocks in one audio frame.<br>BCK = 32 FS~512 FS |

### 8.1.1.15 CLKDET_STATUS REGISTER (OFFSET = 39H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 42. CLKDET_STATUS Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | BCK_OVR_UNR | PCLK_OVR_UNR | PLL_LOCK | BCLK_HALT | BCLK_RATIO_ERR | FS_ERR |
| R/W | | R | R | R | R | R | R |

Table 43. CLKDET_STATUS Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | RESERVED | R/W | 00 | Reserved |
| 5 | BCK_OVR_UNR | R | 0 | This bit indicates whether the BCLK is overrate or underrate |
| 4 | PCLK_OVR_UNR | R | 0 | This bit indicates whether the PLL is overrate or underrate |
| 3 | PLL_LOCK | R | 0 | This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. |
| 2 | BCLK_HALT | R | 0 | This bit indicates whether the BCK is missing or not. |
| 1 | BCLK_RATIO_ERR | R | 0 | This bit indicates whether the BCK is valid or not. The BCK ratio must be stable and in the range of 32-512FS to be valid. |
| 0 | FS_ERR | R | 0 | In auto detection mode (reg_fs_cfg=0), this bit indicated whether the audio sampling rate is valid or not. In nonauto detection mode(reg_fs_cfg!=0), Fs error indicates that configured fs is different with detected fs. Even FS Error Detection Ignore is set, this flag will be also asserted. |



### 8.1.1.16 DIG_VOL_LEFT REGISTER (OFFSET = 4CH) [RESET = 30H]

Return to SUMMARY TABLE.

Table 44. DIG_VOL_CTL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PGA_LEFT | | | | | | | |
| R/W | | | | | | | |

Table 45. DIG_VOL_CTR Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:0 | PGA_LEFT | R/W | 00110000 | Left Digital Volume<br>These bits control the left channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.<br>00000000: +24.0 dB<br>00000001: +23.5 dB<br>…<br>00101111: +0.5 dB<br>00110000: 0.0 dB<br>00110001: -0.5 dB<br>…<br>11111110: -103 dB<br>11111111: Mute |

### 8.1.1.17 DIG_VOL_RIGHT REGISTER (OFFSET = 4DH) [RESET = 30H]

Return to SUMMARY TABLE.

Table 46. DIG_VOL_CTL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PGA_RIGHT | | | | | | | |
| R/W | | | | | | | |

Table 47. DIG_VOL_CTR Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:0 | PGA_RIGHT | R/W | 00110000 | Right Digital Volume<br>These bits control the left channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.<br>00000000: +24.0 dB<br>00000001: +23.5 dB<br>…<br>00101111: +0.5 dB<br>00110000: 0.0 dB<br>00110001: -0.5 dB<br>…<br>11111110: -103 dB<br>11111111: Mute |

### 8.1.1.18 DIG_VOL_CTRL2 REGISTER (OFFSET = 4EH) [RESET = 0X33]

Return to SUMMARY TABLE.

Table 48. DIG_VOL_CTRL2 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PGA_RAMP_DOWN_SPEED | | PGA_RAMP_DOWN_STEP | | PGA_RAMP_UP_SPEED | | PGA_RAMP_UP_STEP | |
| R/W | | | | | | | |

Table 49. DIG_VOL_CTRL2 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | PGA_RAMP_DOWN_SPEED | R/W | 00 | Digital Volume Normal Ramp Down Frequency<br>These bits control the frequency of the digital volume updates when the volume is ramping down.<br>The setting here is applied to soft mute request.<br>00: Update every 1 FS period<br>01: Update every 2 FS periods<br>10: Update every 4 FS periods<br>11: Directly set the volume to zero (Instant mute) |
| 5:4 | PGA_RAMP_DOWN_STEP | R/W | 11 | Digital Volume Normal Ramp Down Step<br>These bits control the step of the digital volume updates when the volume is ramping down.<br>The setting here is applied to soft mute request, asserted by XSMUTE pin or $0/3$.<br>00: Decrement by 4 dB for each update<br>01: Decrement by 2 dB for each update<br>10: Decrement by 1 dB for each update<br>11: Decrement by 0.5 dB for each update |
| 3:2 | PGA_RAMP_UP_SPEED | R/W | 00 | Digital Volume Normal Ramp Up Frequency<br>These bits control the frequency of the digital volume updates when the volume is ramping up.<br>The setting here is applied to soft unmute request, asserted by XSMUTE pin or $0/3$.<br>00: Update every 1 FS period<br>01: Update every 2 FS periods<br>10: Update every 4 FS periods<br>11: Directly restore the volume (Instant unmute) |
| 1:0 | PGA_RAMP_UP_STEP | R/W | 11 | Digital Volume Normal Ramp Up Step<br>These bits control the step of the digital volume updates when the volume is ramping up.<br>The setting here is applied to soft unmute request, asserted by XSMUTE pin or $0/3$.<br>00: Increment by 4 dB for each update<br>01: Increment by 2 dB for each update<br>10: Increment by 1 dB for each update<br>11: Increment by 0.5 dB for each update |

### 8.1.1.19 DIG_VOL_CTRL3 REGISTER (OFFSET = 4FH) [RESET = 0X30]

Return to SUMMARY TABLE.

Table 50. DIG_VOL_CTRL3 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FAST_RAMP_DOWN_SPEED | | FAST_RAMP_DOWN_STEP | | RESERVED | | | |
| R/W | | | | | | | |

Table 51. DIG_VOL_CTRL3 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | FAST_RAMP_DOWN_SPEED | R/W | 00 | Digital volume emergency ramp down frequency<br>These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.<br>00: Update every 1FS period<br>01: Update every 2FS periods<br>10: Update every 4FS periods<br>11: Directly set the volume to zero (Instant mute) |

| | | | | |
|---|---|---|---|---|
| 5:4 | FAST_RAMP_DOWN_STEP | R/W | 11 | Digital volume emergency ramp down step<br>These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.<br>00: Decrement by 4dB for each update<br>01: Decrement by 2dB for each update<br>10: Decrement by 1dB for each update<br>11: Decrement by 0.5dB for each update |
| 3:0 | RESERVED | R/W | 0000 | Reserved |

### 8.1.1.20 ANA_CTRL REGISTER (OFFSET = 53H) [RESET = 0X49]

Return to SUMMARY TABLE.

Table 52. ANA_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BW | | | | | | | |
| RW | | | | | | | |

Table 53. ANA_CTRL Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:0 | Bandwidth | R/W | 0x49 | Bandwidth depends on Fsw:<br>BD mode:<br>Fsw=260kHz: 0xCC;<br>Fsw=384kHz: 0x98;<br>Fsw=480kHz:0x78;<br>Fsw=768kHz: 0x48;<br><br>1SPW mode:<br>Fsw=260kHz: 0xFC;<br>Fsw=384kHz: 0xDC;<br>Fsw=480kHz:0xBC;<br>Fsw=768kHz: 0x88; |

### 8.1.1.21 AGAIN REGISTER (OFFSET = 54H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 54. AGAIN Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | ANA_GAIN | | | | |
| R/W | | | | | | | |

Table 55. AGAIN Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:5 | RESERVED | R/W | 000 | Reserved |
| 4:0 | ANA_GAIN | R/W | 00000 | Analog Gain Control<br>This bit controls the right channel analog gain.<br>00000: 0 dB<br>00001: -0.5db<br>…...<br>11111: -15.5 dB |



### 8.1.1.22 AGAIN REGISTER (OFFSET = 56H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 56. AGAIN Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | ANA_GAIN | | | | |
| R/W | | | | | | | |

Table 57. AGAIN Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | BW_halfc | R/W | 0 | Classd bandwidth control, half LPF capacitor |
| 6:0 | Reserved | R/W | 00000 | Reserved. |

### 8.1.1.23 BQ_WR_CTRL1 REGISTER (OFFSET = 5CH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 58. BQ_WR_CTRL1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | BQ_WR_FIRST_COEF |
| R/W | | | | | | | |

Table 59. BQ_WR_CTRL1 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7-1 | RESERVED | R/W | 0000000 | Reserved |
| 0 | BQ_WR_FIRST_COEF | R/W | 0 | Indicate the first coefficient of a BQ is starting to write. |

### 8.1.1.24 GPIO0 REGISTER (OFFSET = 62H) [RESET = 2EH]

Return to SUMMARY TABLE.

Table 60. GPIO0 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | ADR_Dir | GPIO0 function | | | | |
| RW | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 61. GPIO0_ADR Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | Reserved | R/W | 0h | Reserved |
| 5 | ADR_Dir | R/W | 1h | 1: GPIO as output.<br>0: GPIO as input. |
| 4:0 | GPIO0 | R/W | 0Eh | 00011: digital input as Hiz<br>01000: open drain output as fault warning;<br>01100: Sdout<br>01110: as fault pin<br>11001: digital input as mute<br><br>Others: reserved |

### 8.1.1.25 GPIO1 REGISTER (OFFSET = 63H) [RESET = 00H]

Return to SUMMARY TABLE.

Table 62. GPIO1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | ADR_Dir | GPIO1 function | | | | |
| RW | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 63. DSP_MISC Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | Reserved | R/W | 0h | Reserved |
| 5 | ADR_Dir | R/W | 0h | 1: GPIO as output.<br>0: GPIO as input. |
| 4:0 | GPIO1 | R/W | 0h | 00011: digital input as Hiz<br>01000: open drain output as fault warning;<br>01100: Sdout<br>01110: as fault pin<br>11001: digital input as mute<br><br>Others: reserved |

### 8.1.1.26 GPIO2 REGISTER (OFFSET = 64H) [RESET = 2CH]

Return to SUMMARY TABLE.

Table 64. GPIO2 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | ADR_Dir | GPIO0 function | | | | |
| RW | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 65. DSP_MISC Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | Reserved | R/W | 0h | Reserved |
| 5 | ADR_Dir | R/W | 1h | 1: GPIO as output.<br>0: GPIO as input. |
| 4:0 | GPIO2 | R/W | 0Ch | 00011: digital input as Hiz<br>01000: open drain output as fault warning;<br>01100: Sdout<br>01110: as fault pin<br>11001: digital input as mute<br><br>Others: reserved |

### 8.1.1.27 DIE_ID REGISTER (OFFSET = 67H) [RESET = 0H]

Return to SUMMARY TABLE.

Table 66. DIE_ID Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DIE_ID | | | | | | | |
| RO | | | | | | | |

Table 67. DIE_ID Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:0 | DIE_ID | RO | 0 | Die ID of the device |

### 8.1.1.28 PHASE_CTRL REGISTER (OFFSET = 6AH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 68. PHASE_CTR Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SYNC_MODE | | | | RCG_INPHASE | RCG_PHASE_SEL | | |
| R/W | | | | | | | |

Table 69. PHASE_CTR Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:4 | SYNC_MODE | R/W | 0000 | synching mode:<br>4'h0: no phase sync<br>4'hD: GPI phase sync<br>4'hE: reg phase sync<br>4'hF: Irclk phase sync |
| 3 | RAMP_PHASE_SEL | R/W | 00 | selects the phase of Ch2:<br>0: ph_ch2 = ph_ch1 + 180 deg<br>1: ph_ch2 = ph_ch1 |
| 2:0 | I2S_SYNC_EN | R/W | 000 | select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, it is recommended set all devices the same RAMP frequency and same spread spectrum. It must be set before driving device into PLAY mode if this feature is needed.<br>Selects the phase of Ch1:<br>0: 0 deg<br>1: 60 deg<br>2: 90 deg<br>3: 120 deg (intended for 3-chip cancellation)<br>4: 180 deg (intended for 2-chip cancellation)<br>5: 240 deg (intended for 3-chip cancellation)<br>6: 270 deg<br>7: 300 deg |

### 8.1.1.29 CHAN_FAULT REGISTER (OFFSET = 70H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 70. CHAN_FAULT Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CBCF_CH2 | CBCF_CH1 | CH1_DC_1 | CH2_DC_1 | CH1_OC_I | CH2_OC_I |
| | | R | | | | | |

Table 71. CHAN_FAULT Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:6 | RESERVED | R | 00 | Reserved |
| 5 | CBCF_CH2 | R | 0 | Right channel cycle by cycle over current fault |
| 4 | CBCF_CH1 | R | 0 | Left channel cycle by cycle over current fault |
| 3 | CH1_DC_1 | R | 0 | Left channel DC fault |
| 2 | CH2_DC_1 | R | 0 | Right channel DC fault |
| 1 | CH1_OC_I | R | 0 | Left channel over current fault |
| 0 | CH2_OC_I | R | 0 | Right channel over current fault |

### 8.1.1.30 GLOBAL_FAULT1 REGISTER (OFFSET = 71H) [RESET = 0H]

Return to SUMMARY TABLE.

Table 72. GLOBAL_FAULT1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OTF | Reserved | OTP_UERR | OTP_CERR | PDROP | CLKF | POV | PUV |
| R | | | | | | | |

Table 73. GLOBAL_FAULT1 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | OTP | R | 0 | 1: over temperature error |
| 6 | Reserved | R | 0 | Reserved |
| 5 | OTP_UERR | R | 0 | 1: OTP uncorrectable error |
| 4 | OTP_UERR | R | 0 | 1: OTP correctable error |
| 3 | PDROP | R | 0 | 1: PVDD drop |
| 2 | CLKF | R | 0 | 1: clock fault |
| 1 | POV | R | 0 | 1: PVDD Over-voltagew fault |
| 0 | PUV | R | 0 | 1: PVDD Under-voltage fault |

### 8.1.1.31 WARNING1 (OFFSET = 72H) [RESET = 0H]

Return to SUMMARY TABLE.

Table 74. WARNING1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLAMP_CH1 | CLAMP_CH2 | Reserved | | | | | OTSD_I |
| R | | | | | | | |

Table 75. WARNING1 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | CLAMP_CH1 | R | 0 | Left channel clamp warning |
| 6 | CLAMP_CH2 | R | 0 | Right channel clamp warning |
| 5:1 | Reserved | R | 00000 | Reserved |
| 0 | OTSD_I | R | 0 | Over temperature shut down fault |

### 8.1.1.32 WARNING2 (OFFSET = 73H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 76.OT_WARNING Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLIP_CH1 | CLIP_CH2 | CBCW_CH1 | CBCW_CH2 | OTW_LEVEL4 | OTW_LEVEL3 | OTW_LEVEL2 | OTW_LEVEL1 |
| R | | | | | | | |

Table 77.OT_WARNING Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | CLIP_CH1 | R | 0 | Left channel clip warning |
| 6 | CLIP_CH2 | R | 0 | Right channel clip warning |
| 5 | CBCW_CH1 | R | 0 | Left channel cycle by cycle over current warning |
| 4 | CBCW_CH2 | R | 0 | Right channel cycle by cycle over current warning |
| 3 | OTW_LEVEL4 | R | 0 | OT Warning 146 |
| 2 | OTW_LEVEL3 | R | 0 | OT Warning 135 |
| 1 | OTW_LEVEL2 | R | 0 | OT Warning 125 |
| 0 | OTW_LEVEL1 | R | 0 | OT Warning 113 |

### 8.1.1.33 PIN_CONTROL1 REGISTER (OFFSET = 74H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 78. PIN_CONTROL1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MASK_OTF | MASK_PDROP | MASK_CLIP | MASK_CLKF | MASK_PUV | MASK_POV | MASK_DC | MASK_OC |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 79. PIN_CONTROL1 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | MASK_OTF | R/W | 0 | Mask OTSD fault report |
| 6 | MASK_PDROP | R/W | 0 | Mask PVDD drop fault report |
| 5 | MASK_CLIP | R/W | 0 | Mask clip fault report |
| 4 | MASK_CLKF | R/W | 0 | Mask clock fault report |
| 3 | MASK_PUV | R/W | 0 | Mask PVDD UV fault report |
| 2 | MASK_POV | R/W | 0 | Mask PVDD OV fault report |
| 1 | MASK_DC | R/W | 0 | Mask DC fault report |
| 0 | MASK_OC | R/W | 0 | Mask OC fault report |

### 8.1.1.34 PIN_CONTROL2 REGISTER (OFFSET = 75H) [RESET = 0XF8]

Return to SUMMARY TABLE.

Table 80. PIN_CONTROL2 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | LATCH_CBCW | LATCH_CLKF | LATCH_OTF | LATCH_OTW | MASK_OTW | MASK_CBCW | MASK_CBCF |
| R/W | | | | | | | |

Table 81. PIN_CONTROL2 Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 1 | |
| 6 | LATCH_CBCW | R/W | 1 | 1: latch cbcw reported to warningz |
| 5 | LATCH_CLKF | R/W | 1 | 1: latch clkf reported to faultz |
| 4 | LATCH_OTF | R/W | 1 | 1: latch otsd reported to faultz |
| 3 | LATCH_OTW | R/W | 1 | 1: latch otw reported to warningz |
| 2 | MASK_OTW | R/W | 0 | Mask OT warning report |
| 1 | MASK_CBCW | R/W | 0 | Mask CBC warning report |
| 0 | MASK_CBCF | R/W | 0 | Mask CBC fault report |

### 8.1.1.35 MISC_CONTROL REGISTER (OFFSET = 76H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 82. MISC_CONTROL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LATCH_CLKDET_2REG | LATCH_CLIP | LATCH_PVDDF | OTF_AUTOREC_EN | LATCH_PDROP | Reserved | ATCH-CLAMP | ASK_CLAMP |
| R/W | | | | | | | |

Table 83. MISC_CONTROL Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | LATCH_CLKDET_2REG | R/W | 0 | 1: latch detailed clock detections reported to regmap |
| 6 | LATCH_CLIP | R/W | 0 | 1: latch clip reported to warningz |
| 5 | LATCH_PVDDF | R/W | 1 | 1: latch pov/puv reported to faultz |
| 4 | OTF_AUTOREC_EN | R/W | 0 | OTF auto-recovery enable |
| 3 | LATCH_PDROP | R/W | 0 | 1: latch pdrop reported to faultz |
| 2 | Reserved | R/W | 0 | Reserved |
| 1 | ATCH-CLAMP | R/W | 0 | latches clamp reported to warningz |
| 0 | ASK_CLAMP | R/W | 1 | masks clamp reported to warningz |

# 9. 应用和实现

NOTE

The information provided in this section is not part of the AnalogySemi component specification. Hence, AnalogySemi does not warrant its completeness or accuracy. Customers are responsible for determining suitability of components and system functionality for their applications. Validation and testing should be performed prior to design implementation.

## 9.1 自举电容

AU6825 建议使用 0.22uF-0.47uF 的电容用于自举电容。

### 9.1.1 电感选型

It is required that the peak current be smaller than the OCP (over current protection) value which is 5A. There are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to θ.

$$I_{peak\_power\_up} \approx PVDD \times \sqrt{C/L} \times \sin\left(1/\sqrt{L \times C} \times \theta / F_{SW}\right) \quad (1)$$

Where:

θ = 0.5 (BD Modulation), 0.14 (1SPW Modulation), 0.14 (Hybrid Modulation). This formula just provides a rough estimation. It is suggested to measure the start-up current based on LC filter.

Table 84. Peak Current during Power-Up

| PVDD | L (μH) | C (μF) | fsw (kHz) | $I_{peak\_power\_up}$ |
|---|---|---|---|---|
| 24 | 4.7 | 0.68 | 384 | 6.07A (> 5A OCP), not recommended |
| 24 | 4.7 | 0.68 | 768 | 3.25A |
| 24 | 10 | 0.68 | 384 | 3A |
| 24 | 10 | 0.68 | 768 | 1.55A |
| 12 | 4.7 | 0.68 | 384 | 3.32A |
| 12 | 10 | 0.68 | 384 | 1.55A |

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping wil cause PWM duty cycle increase dramatically. This is the worst case and it rarely happens.

$$I_{peak\_clipping} \approx PVDD \times (1 - \theta) / (F_{SW} \times L) \quad (2)$$

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak\_output\_power} \approx \sqrt{2 \times Max\_Output\_Power / R_{Speaker\_Load}} \quad (3)$$

Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation.

It is suggested that inductor's saturation current $I_{SAT}$, be larger than the amplifier's peak current during power-up and play audio.

$$I_{SAT} \geq \max(I_{peak\_power\_up}, I_{peak\_clipping}, I_{peak\_output\_power}) \quad (4)$$

In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in Table 103, to meet datasheet specifications.

The minimum inductance is given in Table 103.

Table 85. LC Filter Recommendation

| VDD (V) | itching Frequency (kHz) | Modulation Scheme | ecommended Minimum Inductance (μH) for LC Filter Design |
|---|---|---|---|
| ≤ 12 | 384 | BD | 4.7μH + 0.68μF |
| > 12 | | | 10μH + 0.68μF |
| ≤ 12 | 384 | 1SPW/Hybrid | 10μH + 0.68μF |
| > 12 | | | 15μH + 0.68μF |

For higher switching frequency ($F_{sw}$), select inductors with minimum inductance to be 384kHz / $F_{sw}$ × L.

### 9.1.2 供电去耦电容设计

推荐使用 0.1uF 电容用于高频滤波，该电容建议尽量靠近 PVDD，此外建议使用不小于 4 个 22uF 容量的电容用于去耦如果是驱动低音，则建议越大越能提供瞬时电流，保证 PVDD 电压稳定。

### 9.1.3 输出 EMI 滤波设计

如果是 EMI 考虑，AU6825 集成了高阶的展频配合硬件电路设计，详细参数设置，请联系类比支持。

## 9.2 TYPICAL APPLICATIONS

### 9.2.1 2.0 (STEREO BTL) SYSTEM

Figure 104 shows the 2.0 (Stereo BTL) system application.

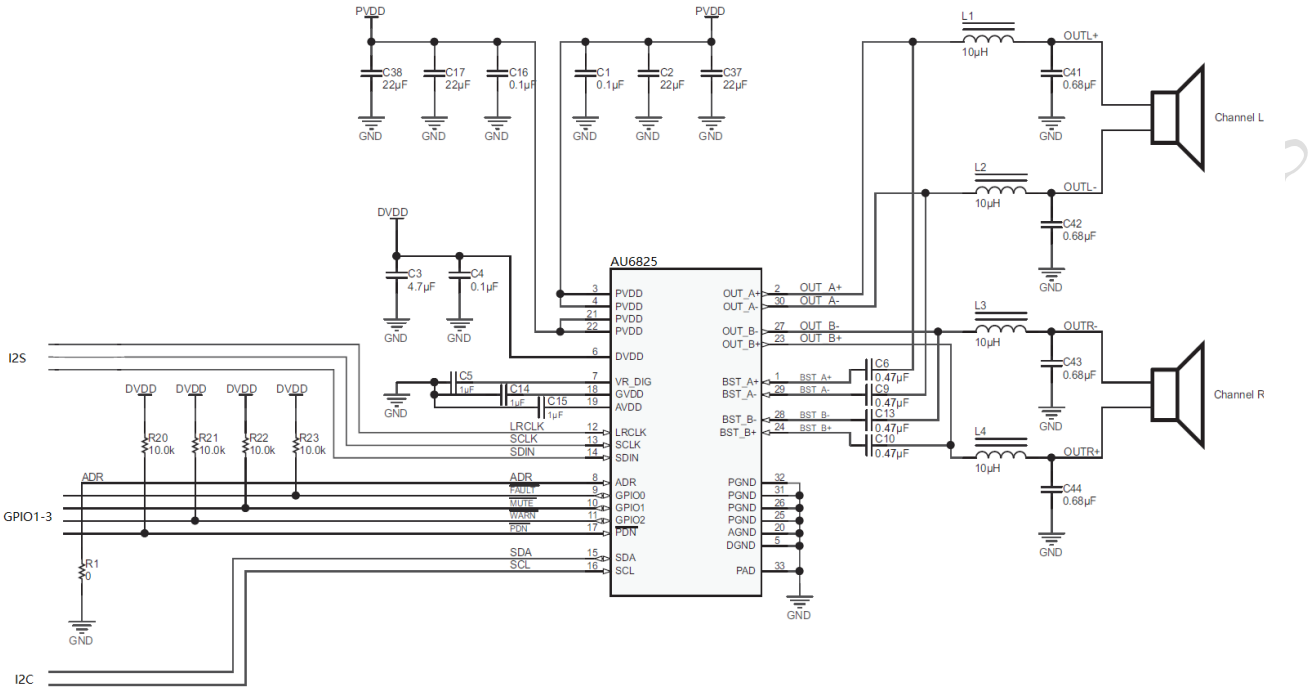
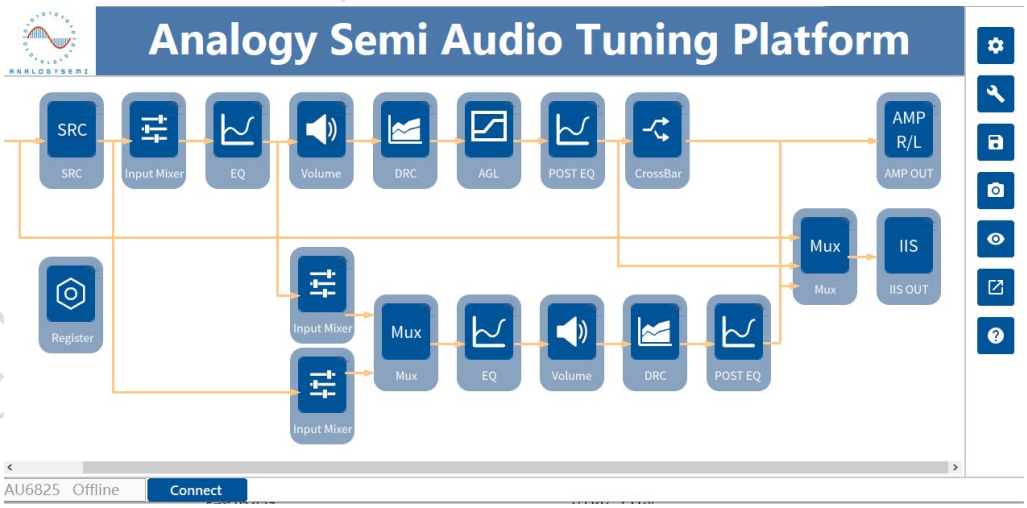



Figure 23. 2.0 (Stereo BTL) System Application Schematic

### 9.2.2 一站式调音软件平台

类比半导体提供一站式软件调试平台 ASATP，可以直接通过输入调试参数，在评估板验证完毕后直接导出驱动配置头文件方便客户软件集成。




类比音频调音平台 ASATP

# 10. 电源供电推荐

The AU6825 device requires two power supplies for proper operation. A high-voltage supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one low- voltage power supply called DVDD is required to power the various low-power portions of the device. Once the device has been initialized, PVDD must keep within the normal operation voltage. Once PVDD is

lower than 3.5V, all registers need re-initialization again.

TBD

Figure 24. Power Supply Function Block Diagram

## 10.1 DVDD SUPPLY

DVDD 支持 3.3V 和 1.8V，通常建议使用 0.1uF 加 4.7uF 作为去耦。

## 10.2 PVDD SUPPLY

PVDD 支持范围为 4.5V-26.4V，一半建议 0.1uF 加 4 个 22uF 以上电容用于去耦。

# 11. 布局

请参考类比半导体评估板。

# 12. PACKAGE INFORMATION

The AU6825 is available in the QFN-32 packages. Figure 118 shows the package view.

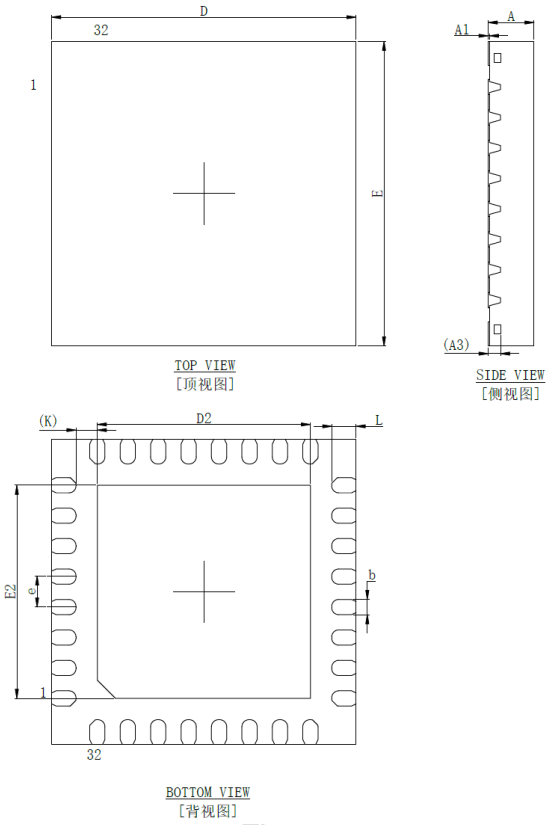



Figure 25. Package View

Table 107 provides detailed information about the dimensions.

Table 86. Dimensions

| SYMBOL | DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.700 | 0.750 | 0.800 |
| A1 | 0.000 | 0.020 | 0.050 |
| A3 | | 0.203 REF | |
| b | 0.200 | 0.250 | 0.300 |
| D | 4.900 | 5.000 | 5.100 |
| E | 4.900 | 5.000 | 5.100 |
| e | | 0.500 BSC | |
| D2 | 3.400 | 3.500 | 3.600 |
| E2 | 3.400 | 3.500 | 3.600 |
| L | 0.300 | 0.400 | 0.500 |
| K | | 0.350 REF | |



# 13. TAPE AND REEL

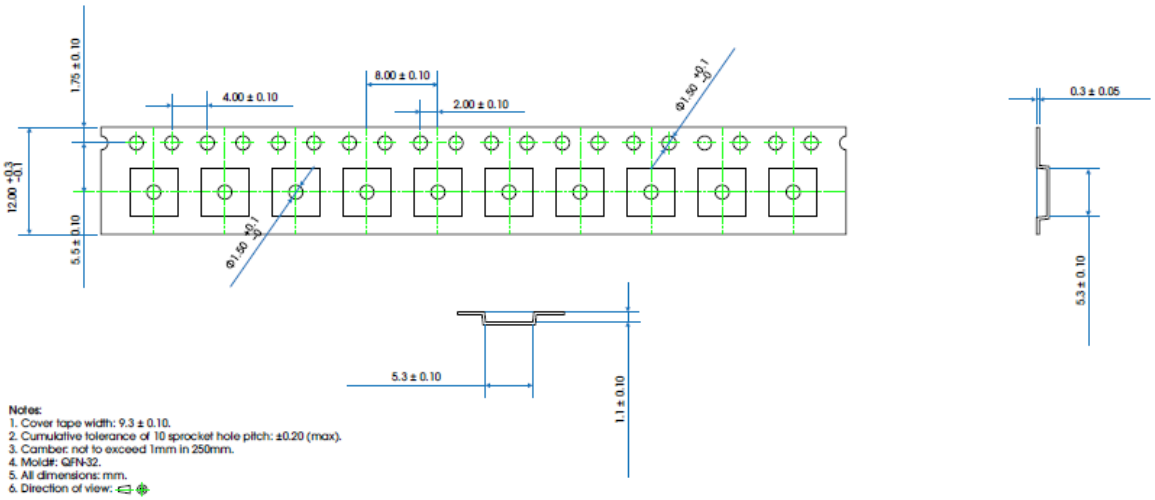


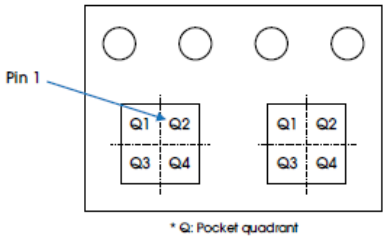

Figure 41. Carrier Tape Drawing

Table 42 provides information about tape and reel.

Table 42. Tape and Reel Information

| PACKAGE TYPE | REEL | QTY/REEL | REEL/ INNER BOX | INNER BOX/ CARTON | QTY/CARTON | INNER BOX SIZE (MM) | CARTON SIZE (MM) |
|---|---|---|---|---|---|---|---|
| QFN-32 5*5 | 13'' | 4000 | 1 | 8 | 32000 | 336*336*448 | 420*355*365 |

Figure 42 shows the product loading orientation—pin 1 is assigned at Q2.



# REVISION HISTORY

| REVISION | DATE | DESCRIPTION |
|---|---|---|
| Rel 0.1 | 22 April 2022 | DRAFT |
| Rel 0.5 | 10 Oct 2022 | Updated spec with features fixed |
| Rel 0.8 | 10 March 2023 | Updated with initial bench data |
| Rel1.0 | 12 April 2023 | Updated with initial data and Chinese wording. |
| Rel 1.1 | 15 Sept 2023 | Updated table 5. |
| Rel 1.1.1 | 25 Nov 2023 | Updated typ errors. |

