2×15W+30W免电感2.1声道D类音频功放

2×15W+30W Inductor Free, 2.1 Channel Class D Amplifier

■ FEATURES

・Output Power
2×12W+24W (VDD=14.5V, R_L=2×8Ω+4Ω, THD+N=1%)
2×15W+30W (VDD=14.5V, R_L=2×8Ω+4Ω, THD+N=10%)
2×8W+16W (VDD=12V, R_L=2×8Ω+4Ω, THD+N=1%)
2×10W+20W (VDD=12V, R_L=2×8Ω+4Ω, THD+N=10%)
・Single Wide Voltage Supply: 4.5V-18V
・Efficiency > 90%
・Spread Switching Frequency For Inductor Free
・Differential / Single-ended Analog Input
・Integrated Self-protection Circuits Including Overvoltage, Undervoltage, Overtemperature, DC-detect, and Overcurrent
・LF and HF Package of QFN6×6-36L

・输出功率
2×12W+24W (VDD=14.5V, R_L=2×8Ω+4Ω, THD+N=1%)
2×15W+30W (VDD=14.5V, R_L=2×8Ω+4Ω, THD+N=10%)
2×8W+16W (VDD=12V, R_L=2×8Ω+4Ω, THD+N=1%)
2×10W+20W (VDD=12V, R_L=2×8Ω+4Ω, THD+N=10%)
・单电源系统，4.5V-18V宽电压输入范围
・超过90%效率，无需散热器
・扩频功能，免电感滤波
・模拟差分/单端输入
・保护功能：过压/过流/过热/欠压异常，直流检测和短路保护
・无铅无卤封装，QFN6×6-36L

■ APPLICATIONS

・Wireless Speakers
・Consumer Audio Applications

・蓝牙/ Wi-Fi音箱
・消费类音频系统

■ DESCRIPTION

HT32201 is a 2.1 channel, efficient, Class-D audio amplifier for driving speakers up to 30W/4Ω+2×15W/8Ω.

Advanced EMI Suppression with Spread Spectrum Control enables the use of inexpensive ferrite bead filters while meeting EMC requirements for system cost reduction.

HT32201 is fully protected against faults with Overvoltage, Undervoltage, Overtemperature, DC-detect, and Overcurrent protection. Faults can be reported to the processor to prevent devices from being damaged.

HT32201是一款高效的2.1声道D类音频功率放大器。在14.5V供电，能够持续提供30W/4Ω+2×15W/8Ω的功率输出。

HT32201具有先进的扩频功能来抑制EMI，使用价格低廉且小体积铁氧体磁珠可满足EMC要求。

此外，HT32201内置关断功能使待机电流最小化，还集成了过压保护、直流保护、短路保护、热保护和电源欠压异常保护等功能，可全面防止出现故障。

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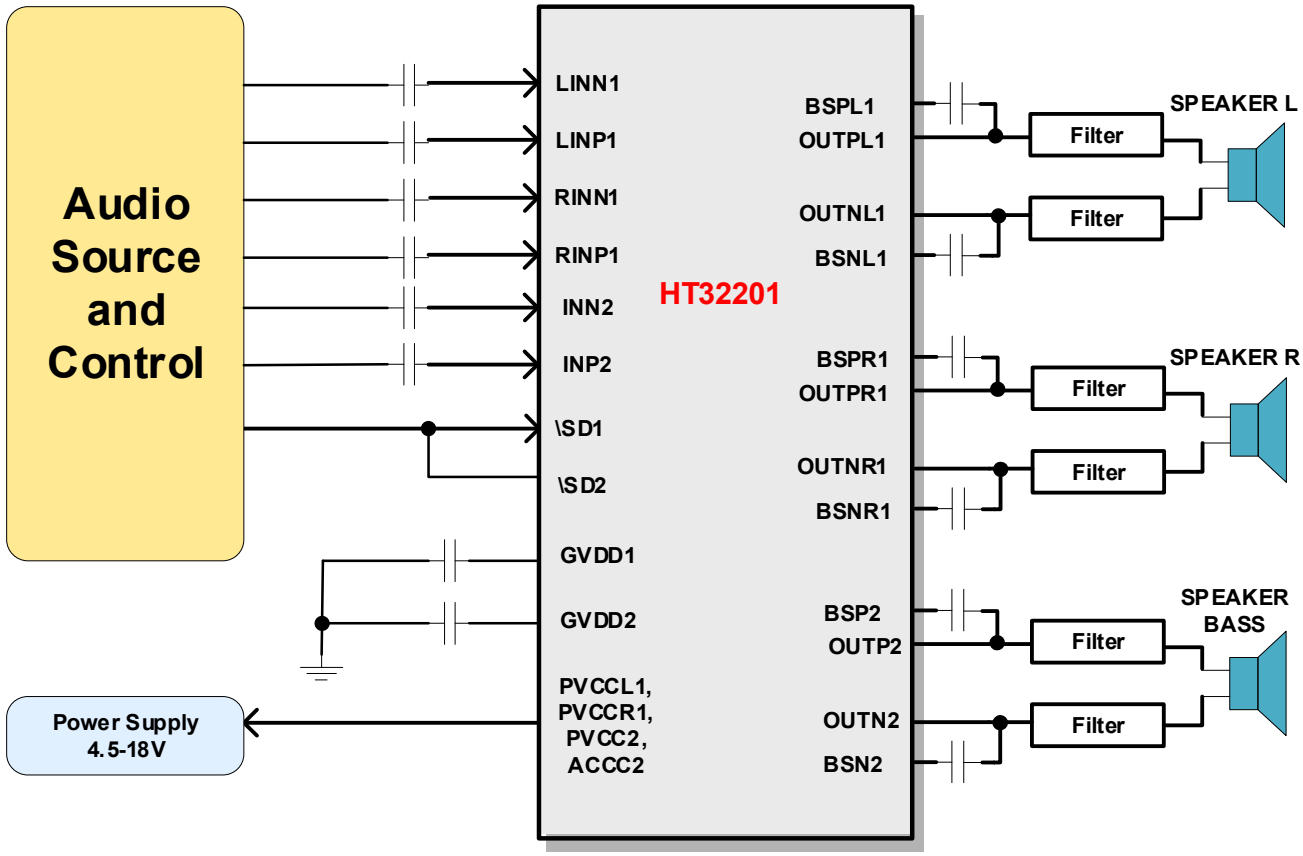
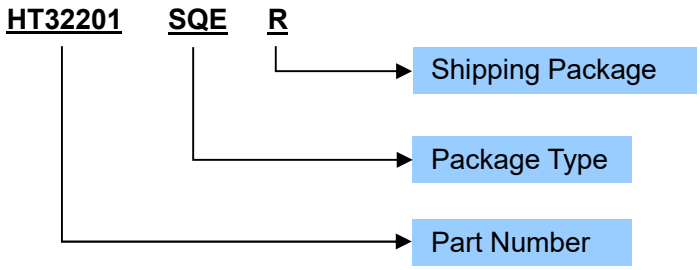
■ TYPICAL APPLICATION



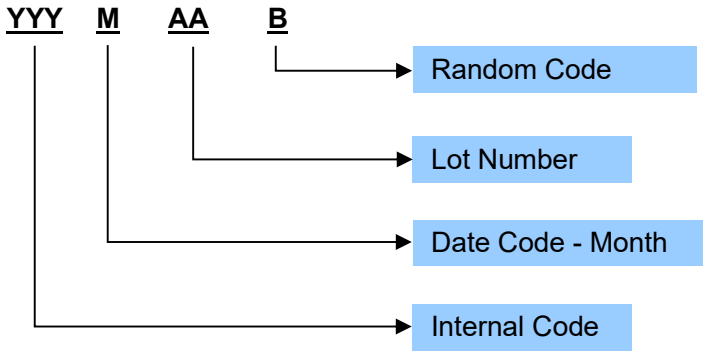
■ ORDERING INFORMATION

Ordering Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HT32201SQER	QFN6×6-36L	HT32201 YYYMAAB[1]	-40℃～85℃	Tape and Reel / 2500pcs

Ordering Number

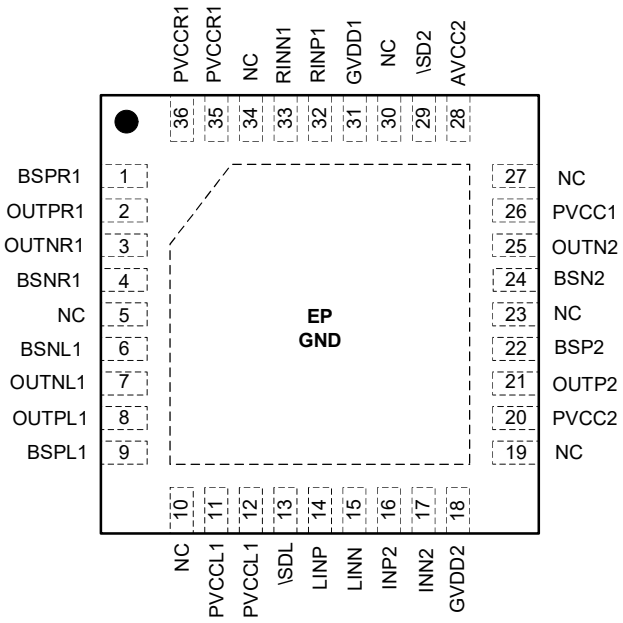


Production Tracking Code



[1] YYYMAAB is production tracking code

■ TERMINAL CONFIGURATION



Top View

■ TERMINAL FUNCTION

Terminal No.	Name	I/O[1]	Description
1	BSPR1	BST	Connection point for the OUTPR1 bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTPR1. OUTPR1自举电容位。
2	OUTPR1	O	Positive pin for differential speaker amplifier output R of channel 1. 1通道右声道输出正端。
3	OUTNR1	O	Negative pin for differential speaker amplifier output R of channel 1. 1通道右声道输出负端。
4	BSNR1	BST	Connection point for the OUTNR1 bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTNR1. OUTNR1-自举电容位。
5, 10, 19, 23, 27, 30, 34	NC	-	No connection, connect GND for better thermal performance. 内部无连接，外部连接到地。
6	BSPL1	BST	Connection point for the OUTPL1 bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTPL1. OUTPL1自举电容位。
7	OUTPL1	O	Negative pin for differential speaker amplifier output L of channel 1. 1通道左声道输出负端。
8	OUTPL1	O	Positive pin for differential speaker amplifier output L of channel 1. 1通道左声道输出正端。
9	BSPL1	BST	Connection point for the OUTPL1 bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTPL1. OUTPL1自举电容位。
11, 12	PVCCL1	P	Power Supply for internal power circuitry of Channel L1. 1通道左声道功率电源。
13	\SD1	I/O	Multi-function pin. When pulled down, place channel 1 in shutdown mode. Also as a speaker amplifier fault terminal, which is pulled LOW when an internal fault of channel 1 occurs, open-drain output. 多功能引脚。当拉低时，通道1处于关闭状态。同时作为错误状态位，通道1发生某些错误时，该引脚拉低。
14	LINP1	I	Positive input terminal for channel L1. 1通道左声道正端输入。
15	LINN1	I	Negative input terminal for channel L1. 1通道左声道负端输入。
16	INP	I	Positive input terminal for channel 2. 2通道正端输入。
17	INN	I	Negative input terminal for channel 2. 2通道负端输入。
18	GVDD2	O	Voltage regulator of channel 2, connect 1uF to GND. 2通道LDO，接1uF到地。
20, 26	PVCC2	P	Power Supply for internal power circuitry of Channel 2. 2通道功率电源。

[1] I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap; OD: Open drain

21	OUTP2	O	Positive pin for differential speaker amplifier output of channel 2. 2通道输出正端。
22	BSP2	BST	Connection point for the OUTP2 bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTP2. OUTP2自举电容位。
24	BSN2	BST	Connection point for the OUTN2 bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTN2. OUTN2自举电容位。
25	OUTN2	O	Negative pin for differential speaker amplifier output of channel 2. 2通道输出负端。
28	AVCC2	P	Analog power supply of channel 2. 2通道模拟电源供电。
29	\SD2	I/O	Multi-function pin. When pulled down, place channel 2 in shutdown mode. Also as a speaker amplifier fault terminal, which is pulled LOW when an internal fault of channel 2 occurs, open-drain output. 多功能引脚。当拉低时，通道2处于关闭状态。同时作为错误状态位，通道2发生某些错误时，该引脚拉低。
31	GVDD1	O	Voltage regulator of channel 1, connect 1uF to GND. 1通道LDO，接1uF到地。
33	RINP1	I	Positive input terminal for channel R1. 1通道右声道正端输入。
34	RINN1	I	Negative input terminal for channel R1. 1通道右声道负端输入。
35,36	PVCCR1	P	Power Supply for internal power circuitry of Channel R1. 1通道右声道功率电源。
EP	GND	G	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground. 既是地，又是散热PAD。

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings[2]

PARAMETER	Symbol	MIN	MAX	UNIT
Supply voltage range (PVDD)	PV_{DD}	-0.3	20	V
Input voltage range (LINP, LINN, RINP, RINN,\SD)	V_I	−0.3	5.8	V
Operating temperature range	T_A	-40	85	℃
Operating junction temperature range	T_J	-40	150	℃
Storage temperature range	T_{STG}	-50	150	℃

● Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage range	V_{DD}	PVDD	4.5		18	V
Operating temperature	T_a		-40	25	85	℃
High-level input voltage	V_{IH}	\SD, Spread on	2.5		5.5	V
Middle-level input voltage	V_{IM}	\SD, Spread off	1.7		2.1	V
Low-level input voltage	V_{IL}	\SD			0.8	V
High-level input voltage	V_{IH}	MODE	1.5		5.5	V
Low-level input voltage	V_{IL}	MODE			0.8	V
Load impedance	R_L	With output filter, OUT1	4	8		Ω
Load impedance	R_L	With output filter, OUT2	2	4		Ω

● DC Electrical Characteristics

Conditions: T_A = 25℃, PV_{DD} = 4.5-18V, Load = 4ohm, unless otherwise specified.

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Class Output Offset Voltage	V_{OS}	V_I = 0V, Gain = 32dB		1.5		mV
Quiescent supply current	I_{DD}	V_{DD} = 12V, No Load		30		mA
Quiescent supply current in SD mode	I_{SD}	V_{DD} = 12V, With Load		22		uA
System Gain	Gain	Rin = 0kΩ		32		dB
		Rin = 8.9kΩ		26		dB
		Rin = 27kΩ		20		dB
Turn-on time	t_{on}	Pull \SD high or power on		80		ms
Turn-off time	t_{off}	Pull \SD low		5		us
Gate drive supply	GVDD			5		V

[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

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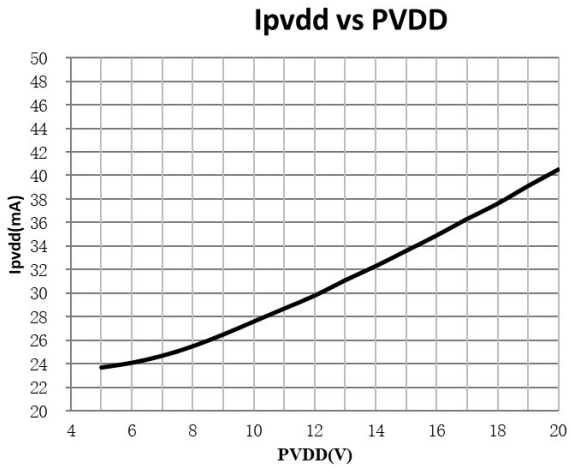
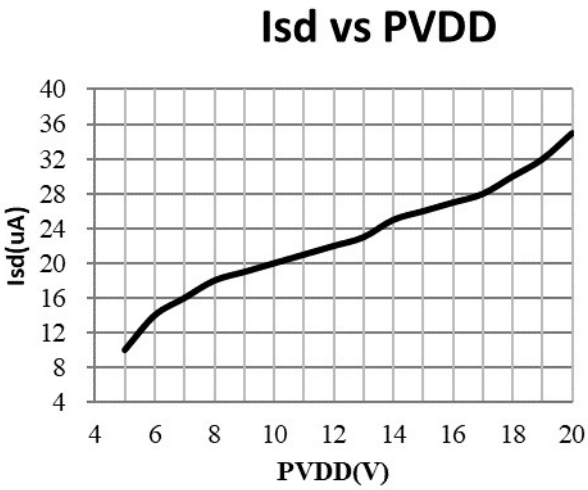
● AC Electrical Characteristics

Conditions: T_A = 25℃, V_{DD} = 4.5-18V, Load = 4Ω + 2×8 Ω, f_{IN} = 1 kHz, Gain = 26dB, C_{IN} = 1uF, 20-20kHz, unless otherwise specified.

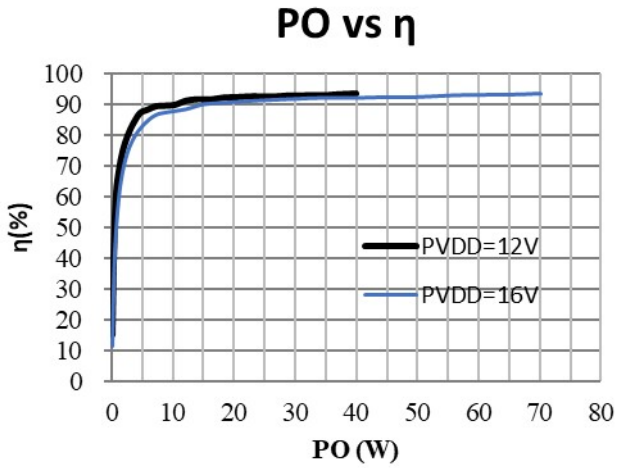
PARAMETER	Symbol	CONDITION		MIN	TYP	MAX	UNIT
Continuous output power	P_O	VDD = 10V, R_L = 4Ω + 2×8 Ω,	THD +N = 1%		10.8+2×5.6		W
			THD+N = 10%		13.5+2×6.9		W
		VDD = 12V, R_L = 4Ω + 2×8 Ω,	THD +N = 1%		15.6+2×8		W
			THD+N = 10%		19.4+2×10		W
		VDD = 14V, R_L = 4Ω + 2×8 Ω	THD +N = 1%		21.1+2×10.9		W
			THD+N = 10%		26.2+2×13.5		W
		VDD = 16V, RL = 4Ω + 2×8 Ω,	THD +N = 1%		27.5+2×14.2		W
			THD+N = 10%		34.1+2×17.6		W
Total harmonic distortion + noise	THD+N	Po = 1W, V_{DD} = 12V, R_L = 4Ω			0.08		%
Efficiency	η	VDD = 12V, THD+N = 10%			90		%
Output integrated noise	V_N	A-weighted, Gain = 26 dB			100		uV
Signal-to-noise ratio	SNR	A-weighted, Gain = 26 dB, Po = 1W/8 Ω			89		dB
Power supply rejection ratio	PSRR	200mVpp 1kHz, Input grounded			-75		dB
Oscillator frequency	f_{osc}				360		kHz
Spread frequency range					±15		kHz
Over temperature protection trigger point	OTP				160		℃
Overtemperature Protection Hysteresis	OTPhys				10		℃
Over current trip point	OCP				7.5		A

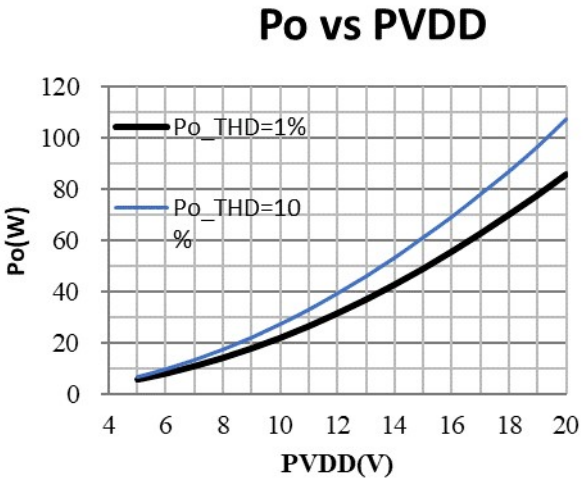
■ TYPICAL OPERATING CHARACTERISTICS



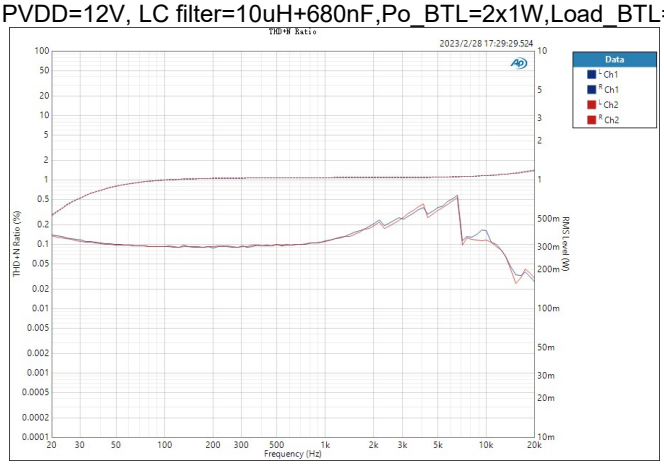


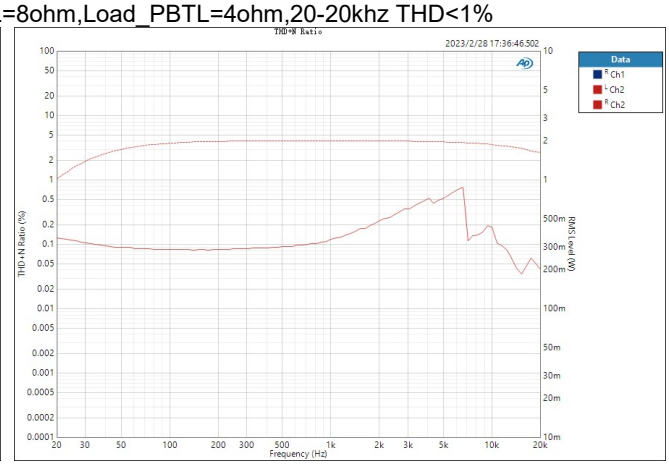
T_A = 25°C, PVDD =12V, f_{IN} = 1 kHz, Load_BTL = 8ohm, Load_PBTL=4ohm, LC filter=10uH+680nF, unless otherwise noted.





PVDD=12V, LC filter=10uH+680nF,Po_BTL=2x1W,Load_BTL=8ohm,Load_PBTL=4ohm,20-20khz THD<1%





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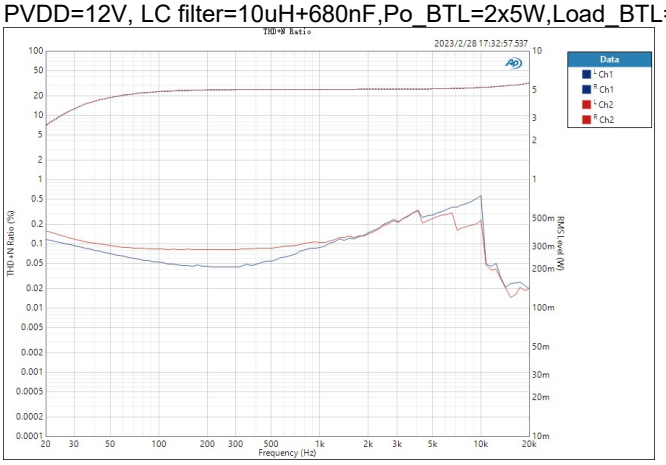
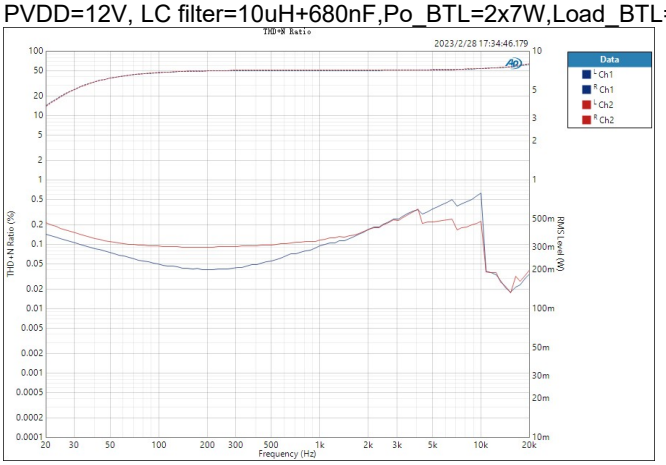
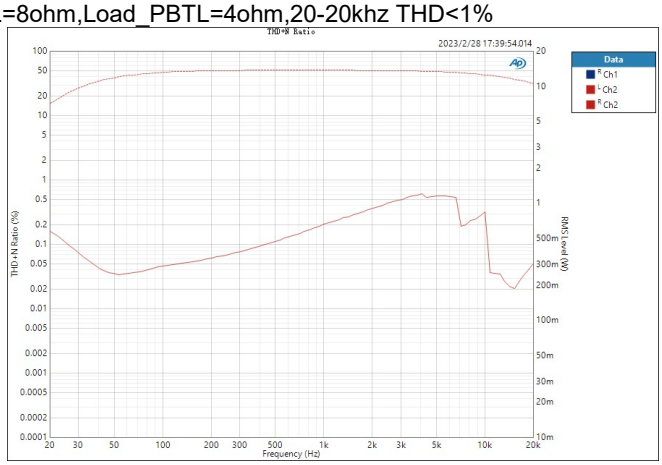


PVDD=12V, LC filter=10uH+680nF,Po_BTL=2x7W,Load_BTL=8ohm,Load_PBTL=4ohm,20-20khz THD<1%





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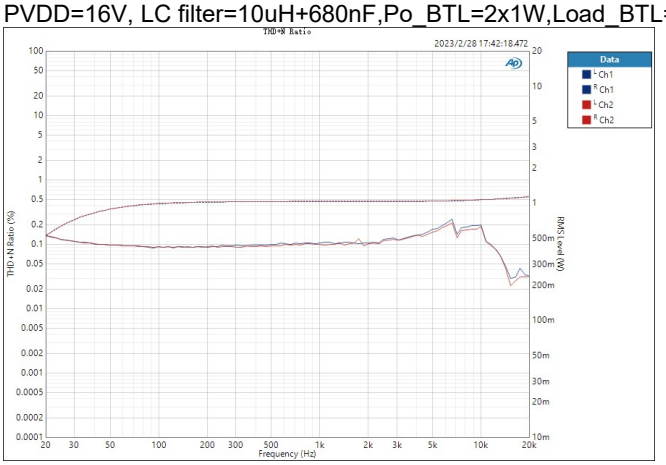
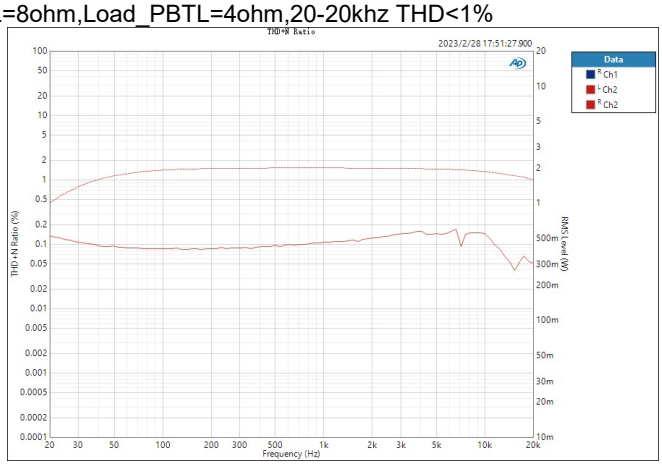
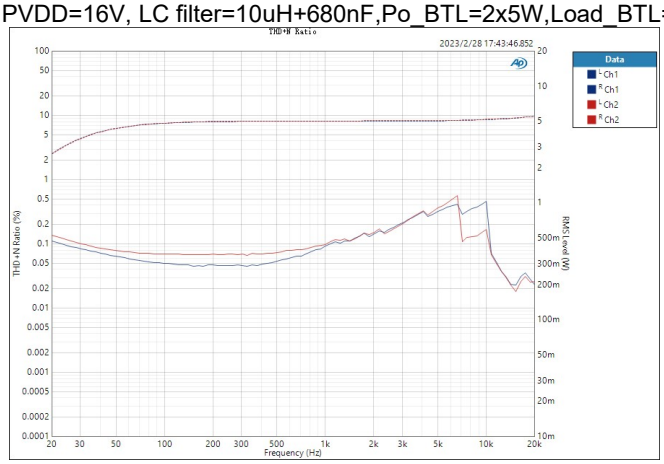
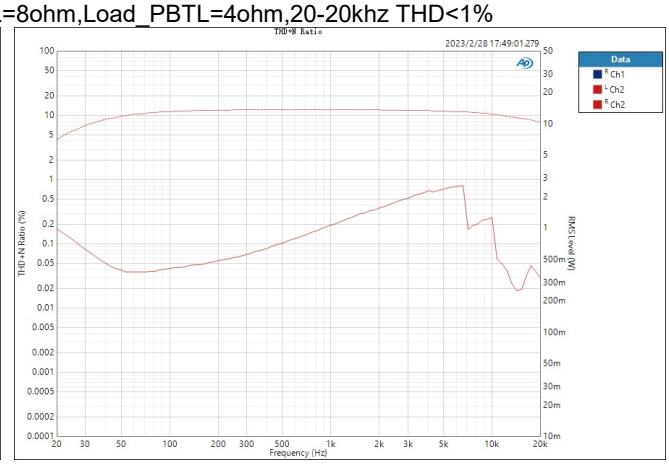


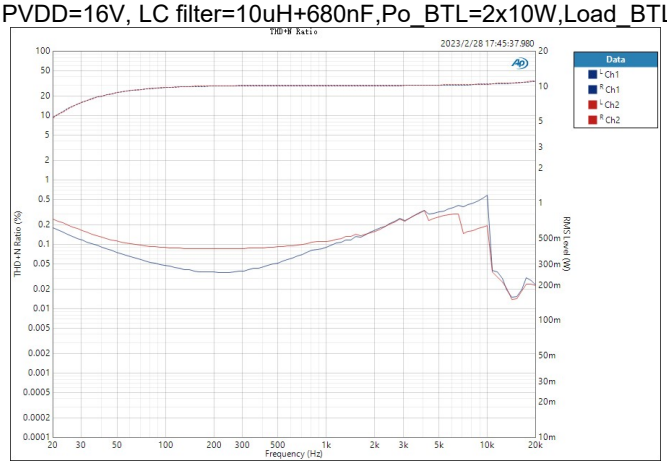


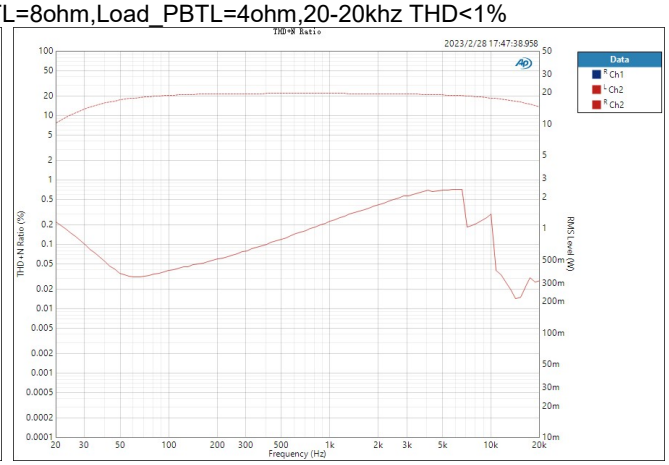
PVDD=16V, LC filter=10uH+680nF,Po_BTL=2x5W,Load_BTL=8ohm,Load_PBTL=4ohm,20-20khz THD<1%



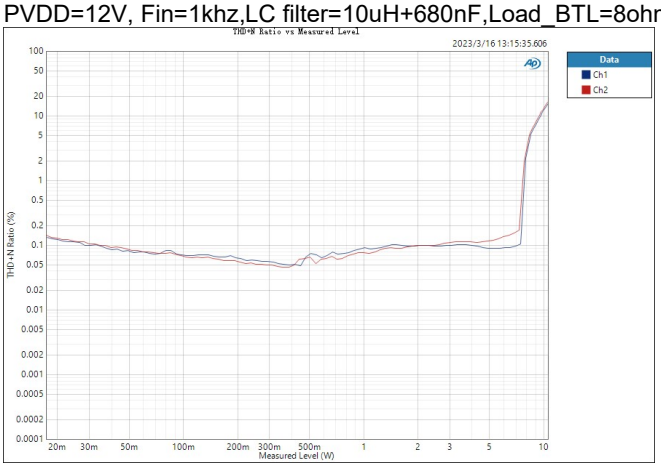


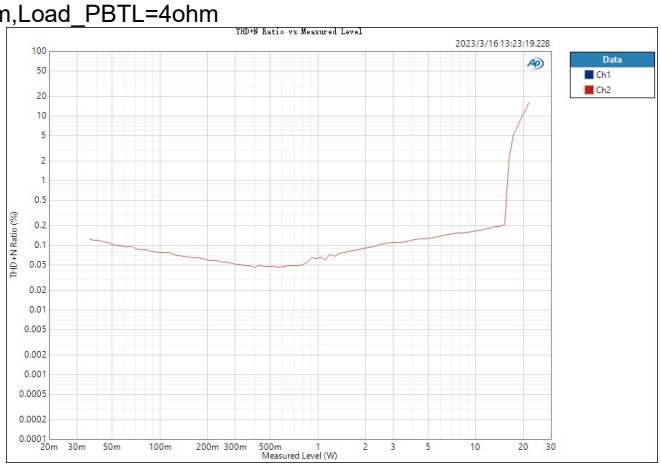
PVDD=16V, LC filter=10uH+680nF,Po_BTL=2x10W,Load_BTL=8ohm,Load_PBTL=4ohm,20-20khz THD<1%



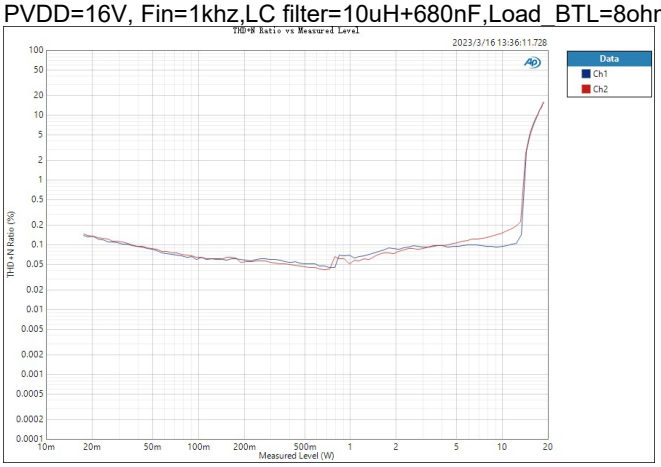


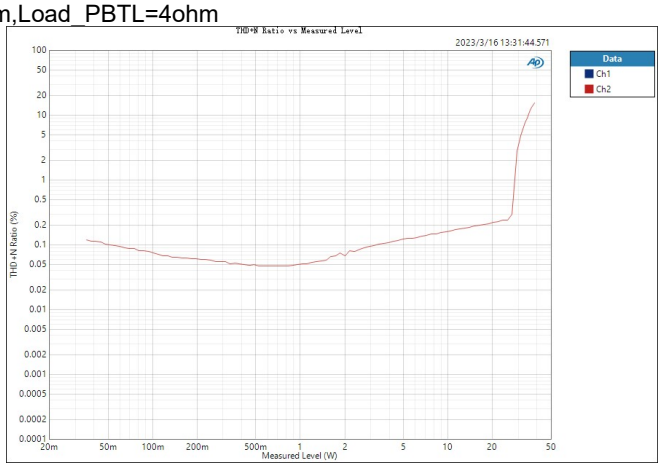
PVDD=12V, Fin=1khz,LC filter=10uH+680nF,Load_BTL=8ohm,Load_PBTL=4ohm





PVDD=16V, Fin=1khz,LC filter=10uH+680nF,Load_BTL=8ohm,Load_PBTL=4ohm





■ APPLICATION INFORMATION

1 Power Supplies

The power supply for the HT32201 only require one voltage from 4.5V to 18V, which supplies the analog circuitry and the power stage.

The PVDD supply feeds internal LDO including GVDD. This LDO output is connected to external pins for filtering purposes, but should not be connected to external circuits. The filtering capacitor for GVDD is recommended to be 1uF.

The PVDD also feeds the power stage of audio amplifier. Filtering capacitors of 100nF//1uF//220uF for PVDD of each channel should be placed close to the PVDD pin.

HT32201 仅需要 1 个电源供电，即在 PVDD 端加 4.5-18V。

GVDD 是内部的 LDO 输出，建议加 1uF 电容到地

每个通道的 PVDD 端建议各加 100nF//1uF//220uF 的并联电容到地。

2 Amplifier Input and Output

2.1 Amplifier Input Configuration

HT32201 is an amplifier with analog input (single-ended or differential). For a differential operation, input signals into IN+ and IN- pins via DC-cut capacitors (CIN). The high pass cut-off frequency of input signal can be calculated by

. The input signal gain is calculated by $Gain \approx R_F / (External\ R_{IN} + Internal\ R_{IN})$. The R_F = 370k, internal R_{IN}=9.6k.

For a single-ended operation, input signals to IN+ pin via a DC-cut capacitor (C_{IN}). IN- pin should be connected to ground via a DC-cut capacitor (with the same value of C_{IN}).

HT32201 支持差分输入或单端输入。

差分输入时，信号经过输入隔直电容 CIN 连接到 IN+和 IN-，高通滤波器截止频率为：

放大倍数为：

$Gain \approx R_F / (External\ R_{IN} + Internal\ R_{IN})$

其中， R_F = 370k, internal R_{IN}=9.6k

单端输入时，信号经输入隔直电容 C_{IN} 连接至 IN+, IN-接相同的输入电容到地。

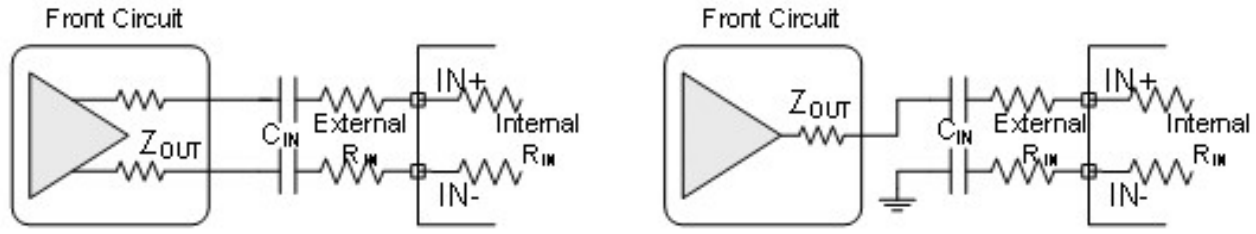


Figure 1 (1) Differential Input; (2) Single-ended Input

2.2 Amplifier Output Configuration

The HT32201 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 10 cm and high power. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the class-D amplifier. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz. Also, the filter capacitor can be increased if necessary, with some impact on efficiency.

HT32201 在很多应用场合，包括大功率、喇叭线长度达到 10cm 条件下，可使用磁珠作为滤波器。对于磁珠的选择，不同材料类型会有不同的表现，关键之一是在 10M ~ 100MHz 内表现。使用磁珠时，可配合使用 1nF 的下地电容，谐振频率应小于 10MHz。

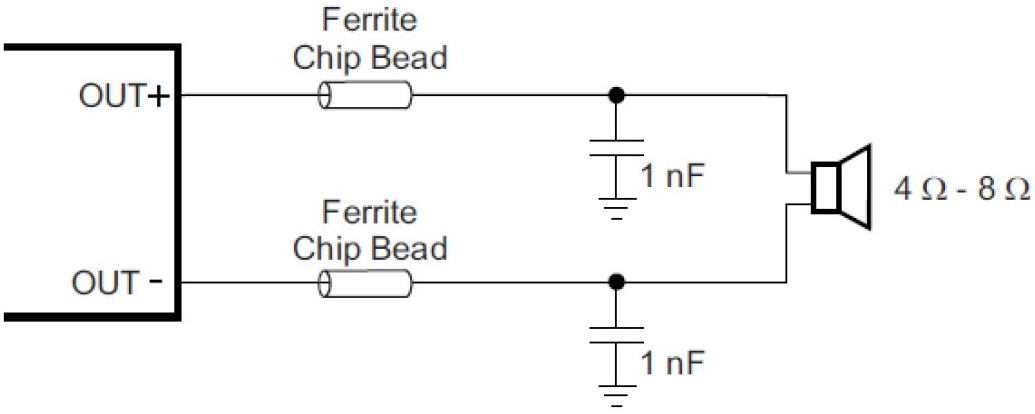


Figure 2 Output Filters with Ferrite Beads

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in the figures below can be used.

在某些条件下，如周边元器件对辐射较为敏感，或 EMI 辐射难以达到标准，输出需要加 LC 滤波器。

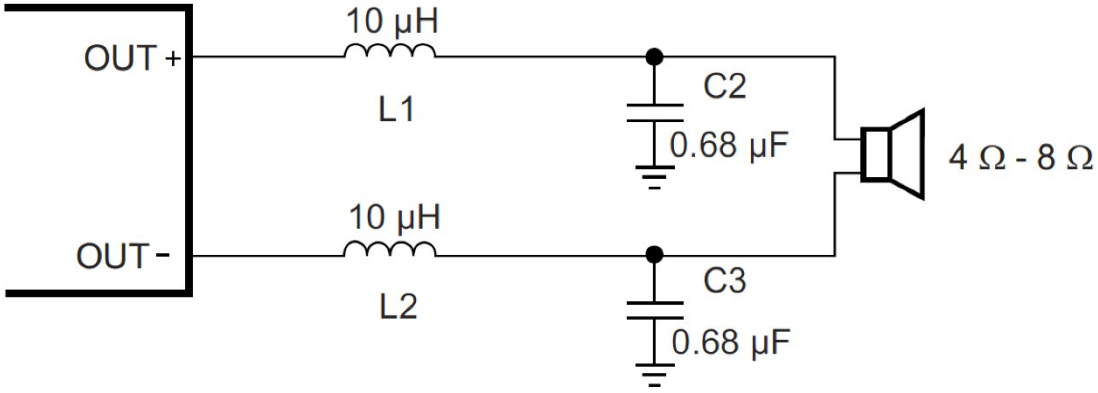


Figure 3 Output Filters with LC

3 Startup, Shutdown

The HT32201 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for power conservation. The \SD input terminal should be held high during normal operation when the amplifier is in use. Pulling \SD low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave \SD unconnected, because amplifier operation would be unpredictable.

For a better power on and power-off pop performance, place the amplifier in the shutdown mode prior to delivering or removing the power supply..

HT32201 具有关断功能，以使芯片进入低功耗状态。当\SD 拉高时，芯片进入工作状态；当\SD 拉低时，芯片进入关断状态。

\SD 不建议悬空，否则可能状态不定。

上下电时，为减小 pop 声，在上、下电前，将功放关闭进入关断状态。

4 Spread Spectrum and De-Phase Control

The HT32201 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM outputs to improve EMI performance. The spread spectrum scheme is internally fixed and by setting the SD pin above 2.5V to turn on.

HT32201具有扩频功能，以提升EMI表现。当关断功能，以使芯片进入低功耗状态。当ENA电压高于2.5V时，该功能开启。

5 Other Functions and Terminals

5.1 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 1uF ceramic capacitor of quality X5R or better, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

功放输出驱动级H桥采用的是NMOS，因此需要自举电容提供更高的栅极电压驱动高端管导通。使用一个1uF,25V以上电容连接于BSxx和对应输出之间。

6 Protection Functions

The HT32201 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, under-voltage, and over-voltage.

HT32201具有一系列保护功能，如短路保护、过温保护、直流保护、欠压保护、过压保护等。

6.1 Over Temperature Protection (OTP)

This is the function to establish the over temperature protection mode when detecting excessive high temperature of HT32201. When the on-die temperature of HT32201 is higher than OTP, the OTP mode is activated, the differential output pin becomes weak low state (a state grounded though resistivity), and the \SD pin is pulled low. When the on-die temperature is then lower than OTP-OTPhys, the chip is resume to work.

HT32201内部高于OTP温度时，芯片OTP保护功能启动，功放关断、\SD拉低。

6.2 DC Detect Protection (DCP)

The HT32201 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. A DC detect fault will be reported on the \SD pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2 Hz.

HT32201具有直流保护功能，以保护可能的喇叭端直流信号。保护功能发生时，\SD拉低，功放关断。

当输出某个通道的差分信号在同一极性的占空比超过60%并持续429ms以上，直流保护功能开启.

6.3 Short-Circuit Protection (OCP) and Automatic Recovery

The HT32201 has protection from over current conditions caused by a short circuit on the output stage. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The short circuit protection fault is reported on the \SD pin as a low state.

When OCP or OTP or DC error is detected, the \SD pin will be pulled low. Because the \SD input is low, it clear the error signal. After a ton time (normally 1.3s), HT32201 will try restart.

当HT32201输出短路而发生过流时，芯片会发生保护，芯片关断，\SD拉低。

当OCP, OTP, DCP发生时，\SD均会被拉低，经过1.3s, HT32201会尝试重新启动.

6.4 Under-Voltage Protection (UVP)

This is the function to establish the under-voltage protection mode when power supply becomes lower than the detection voltage VUVLL, and the protection mode is canceled when the power supply becomes higher than the threshold voltage VUVLH. In the under-voltage protection mode, the differential output pin becomes weak low state (a stage grounded through resistivity). HT32201 will start up within start-up time when the under-voltage protection mode is cancelled.

HT32201具有欠压保护功能，以防止输入电压过低。

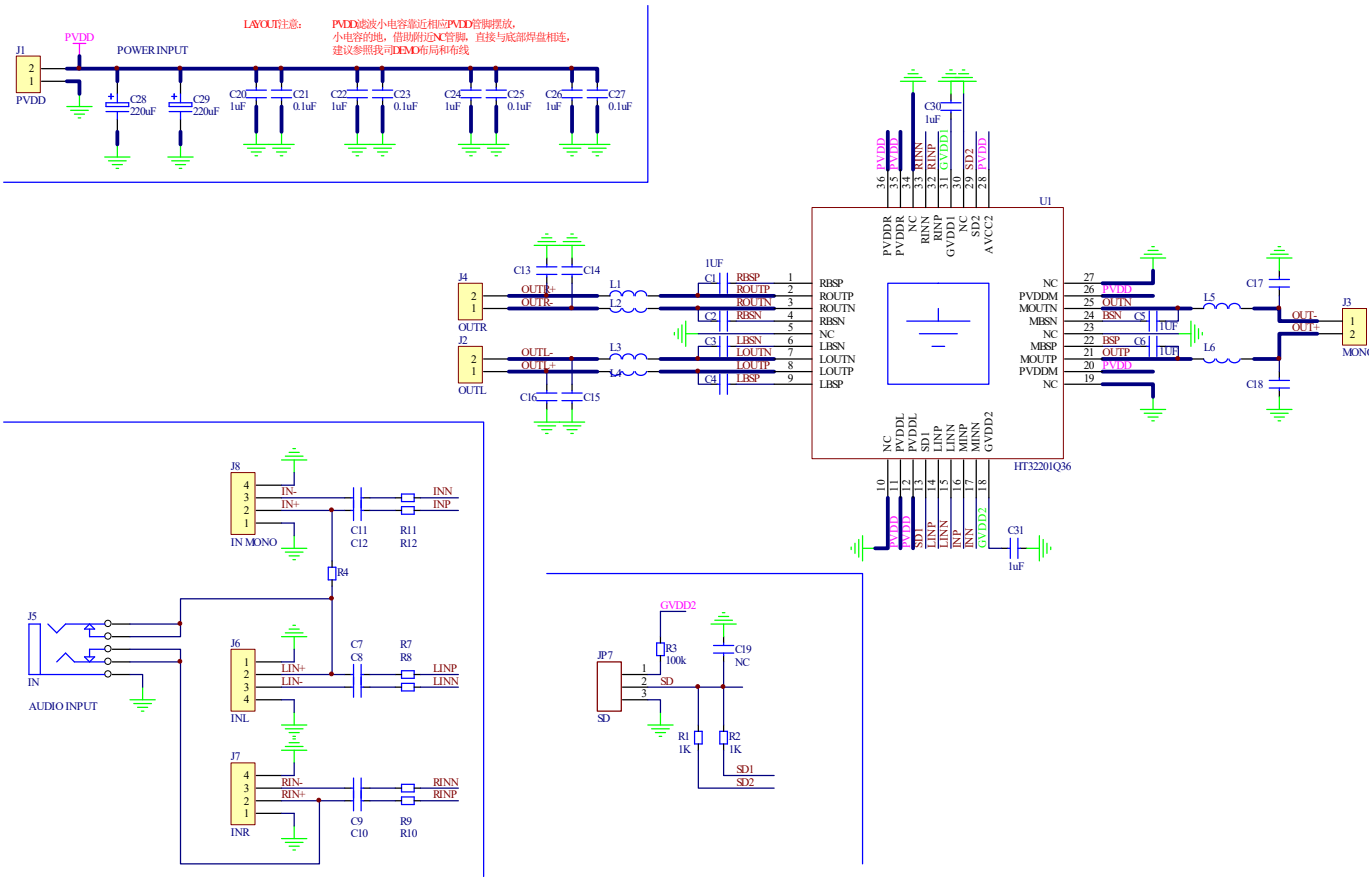
当PVDD小于VUVLL时，欠压保护启动，升压关闭。当PVDD高于VUVLH时，升压重新开启。

6.5 Over-Voltage Protection (OVP)

The HT32201 device monitors the voltage on PVDD voltage threshold. When the voltage on PVDD pin exceeds the over-voltage threshold (28V typ), the OVP circuit puts the device into shutdown mode. The device recovers automatically once the over-voltage condition has been removed.

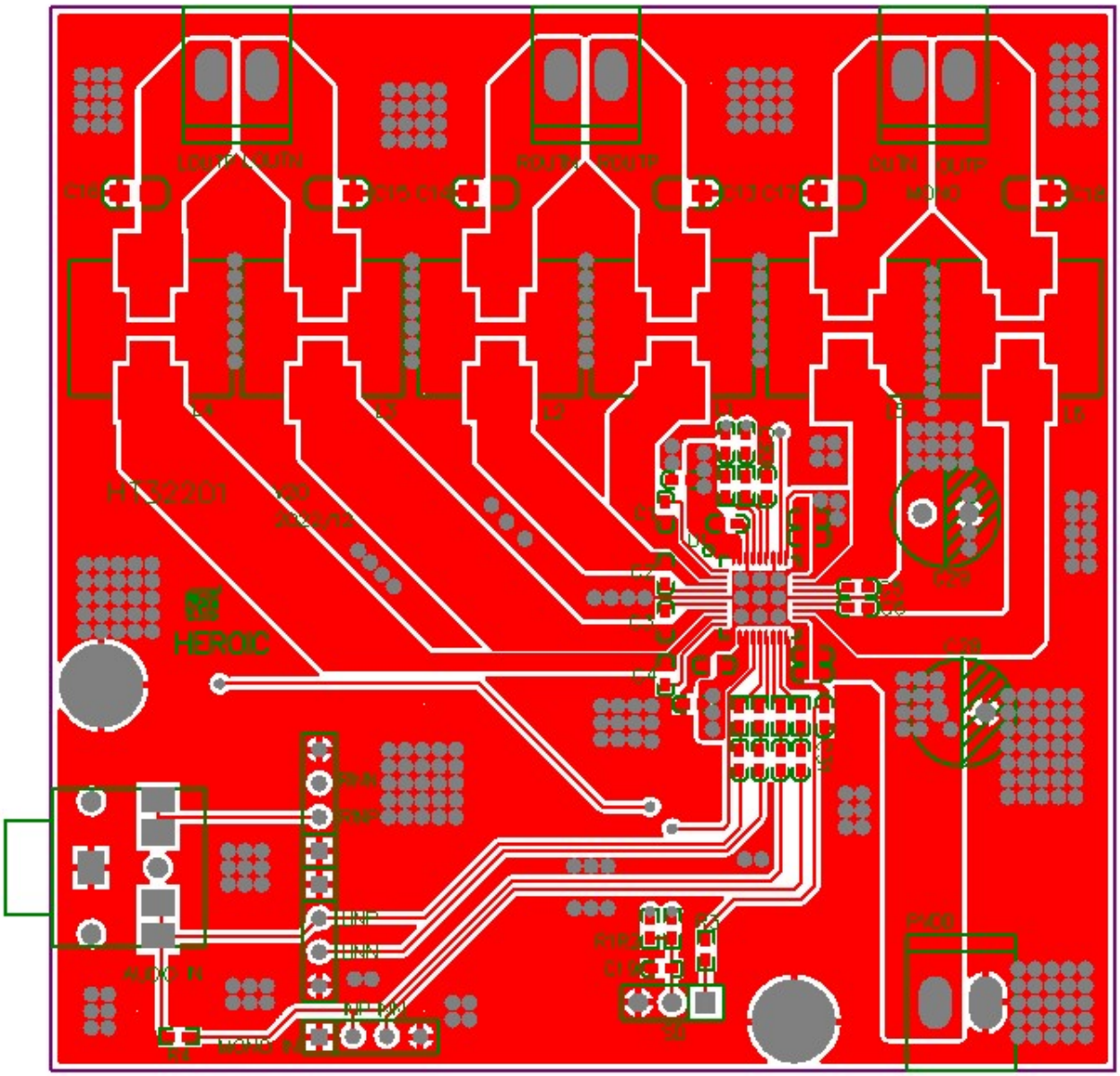
HT32201检测PVDD电压，当电压高于28V时，OVP启动，功放输出关闭。当过压条件撤销，功放自动开启。

7 Typical Circuit Diagram

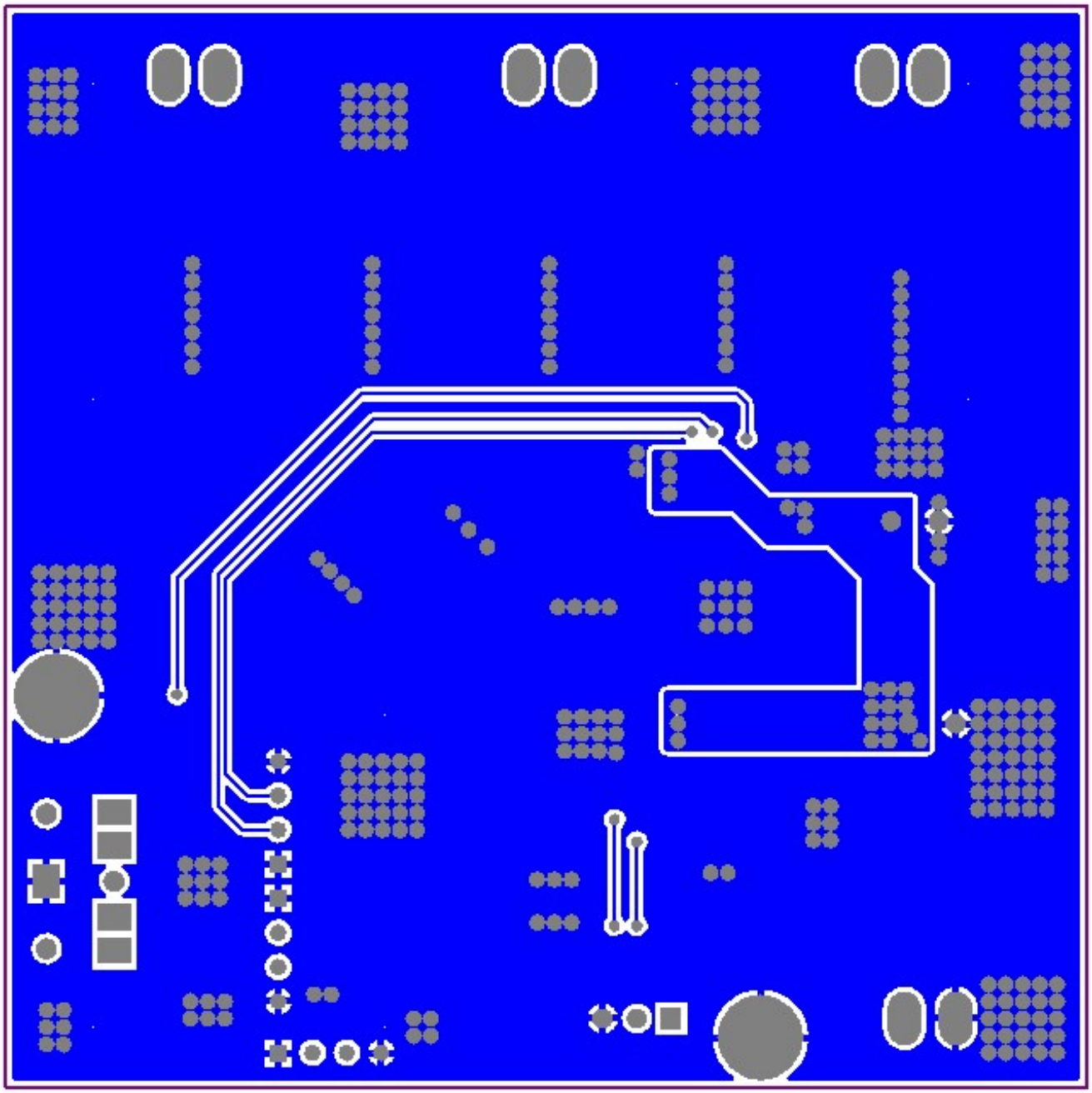


8 PCB Layout

1.1 Top Layer

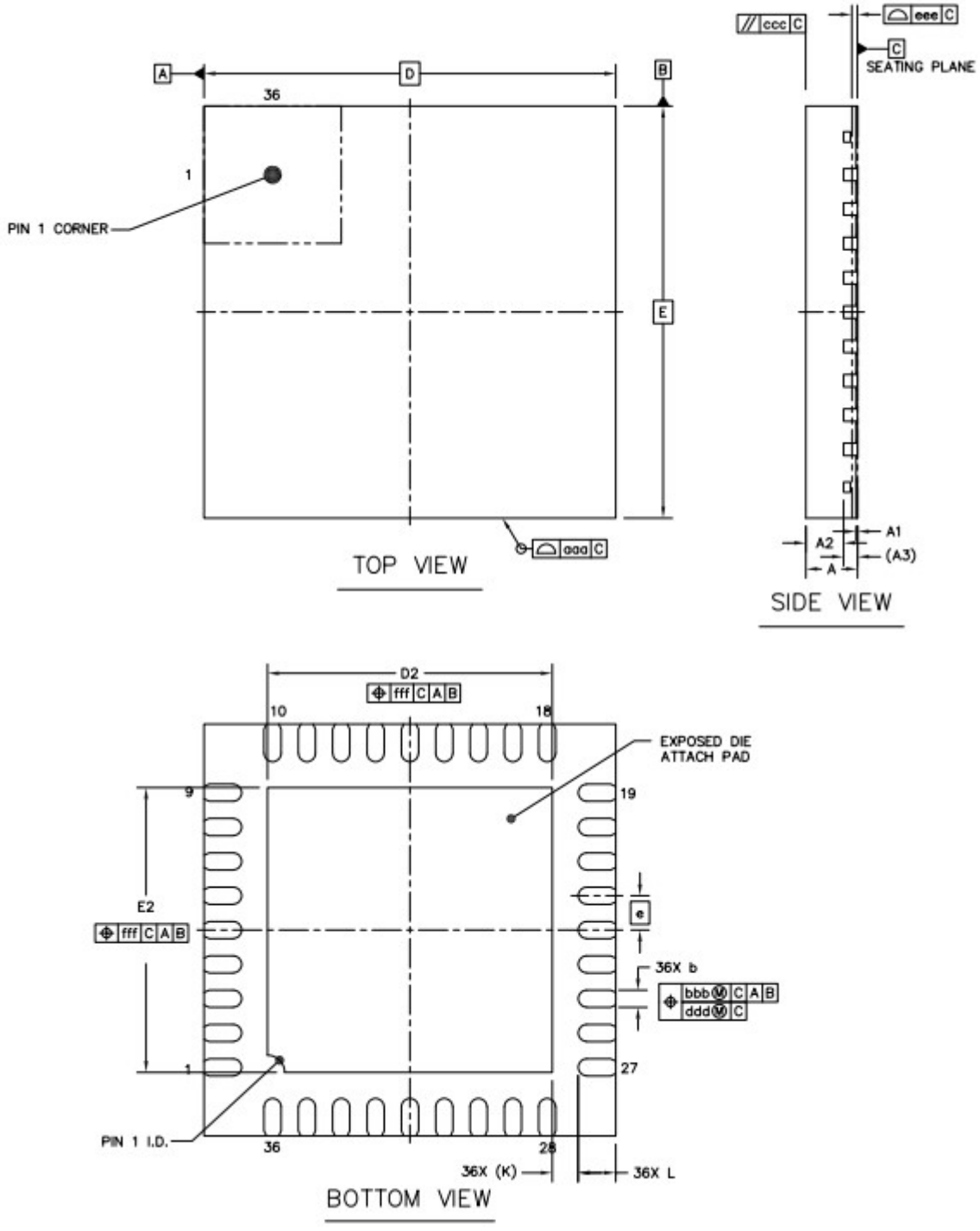


1.2 Bottom Layer



■ PACKAGE OUTLINE

SQE (QFN6×6-36L)



Symbol	Dimensions in Millimeters		
	Min.	NOM	Max.
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2		0.55	
A3	0.203REF.		
D	6BSC		
E	6BSC		
e	0.5BSC		
D2	4.05	4.15	4.25
E2	4.05	4.15	4.25
L	0.45	0.55	0.65
k	0.375REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		

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