内置升压的25W立体声D类音频功放

2×25W Class D Audio Amplifier with Boost Converter

■ FEATURES

- Output Power (f_{IN} = 1kHz, R_L=4Ω)

VBAT = 7.2V, 2×25W (VOUT=14.8V, THD+N= 10%)
VBAT = 3.7V, 2×10W (VOUT=9V, THD+N = 10%)

- Power Supply V_{BAT}: 2.7V~VOUT
- Spread Switching Frequency Function for AMP
- Integrated boost converter: adjustable output voltage VOUT and switch peak current limit
- Over current protection/ Over temperature protection / Overvoltage protection / Low voltage malfunction prevention function with auto recovery
- Pb-free Packages, ETSSOP28

- 输出功率(f_{IN}=1kHz, R_L=4Ω)

双锂电7.2V：2×25W (VOUT=14.8V, THD+N= 10%)
单锂电3.7V：2×10W (VOUT=9V, THD+N = 10%)

- VBAT供电范围：2.7V至VOUT
- D类功放扩频功能
- 内置升压电路：可调节的升压值和升压限流
- 保护功能：过流/过热/欠压异常/过压保护功能
- 无铅无卤封装，ETSSOP28

■ APPLICATIONS

- Smart Speakers
- Wireless Speakers
- Portable Speakers
- 2.1Channel Speakers
- Megaphone
- Portable Gamers

- 智能音响
- 无线音响
- 便携式音箱
- 2.1声道小音箱
- 拉杆音箱
- 便携式游戏机

■ DESCRIPTION

The HT81696 is a stereo Class D audio amplifier integrated a boost converter. With wide input voltage range, HT81696 supports applications with single cell, two cell Lithium batteries, 5V or 12V power supply and so on.

HT81696 built-in boost converter supports selectable output voltage by external resistors for different applications with different power requirements. It also implements an adjustable switching peak current limit function through external resistors.

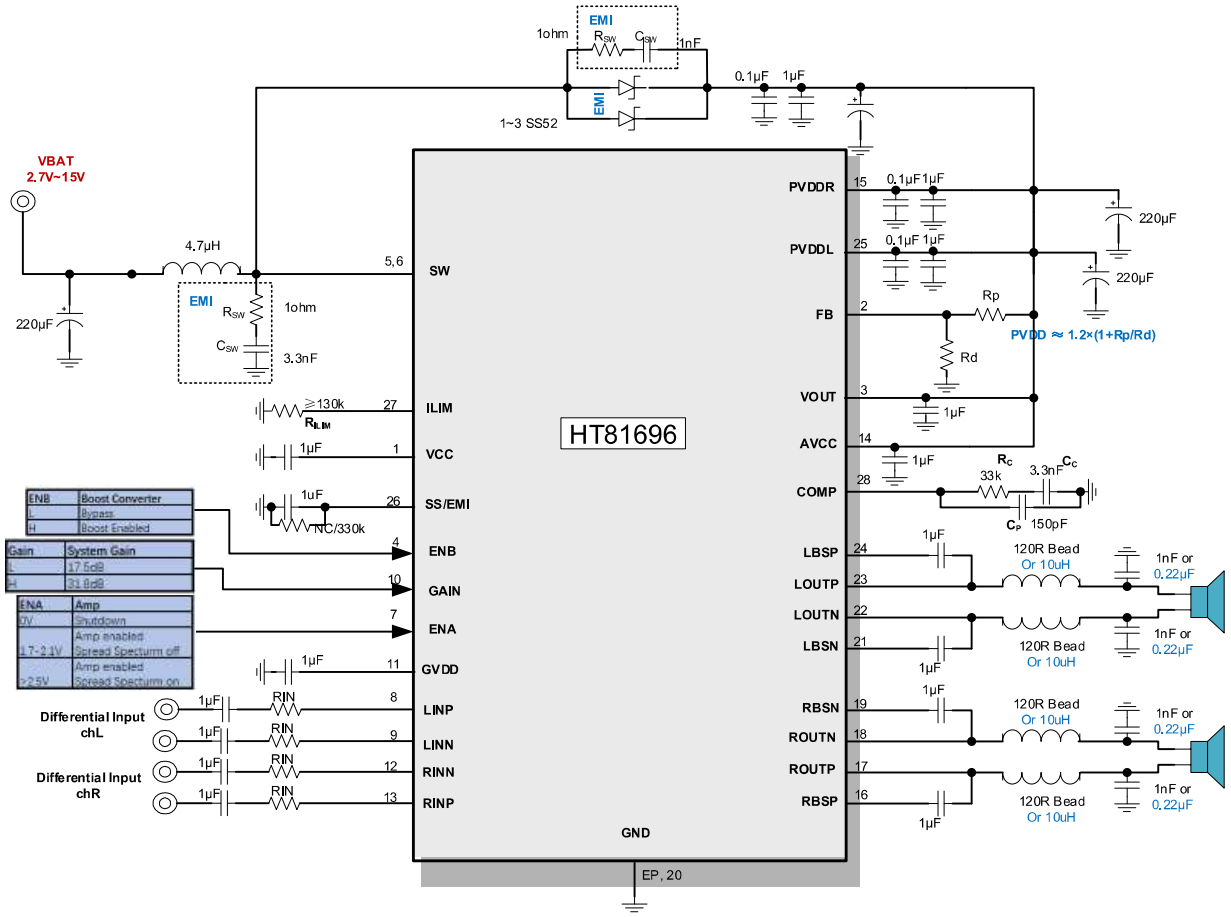
HT81696 has a filter-less modulation circuit which can directly drive speakers. HT81696 can be shut down so that the power consumption can be minimized. As for protection function, over current protection function for speaker output terminals, over temperature protection function, low supply voltage malfunction preventing function and over boost voltage protection are also prepared.

HT81696是一款内置升压的立体声D类音频功率放大器，其支持单节锂电、双节锂电串联、5V、12V等多种输入，升压后的电压提供给功放供电。

HT81696内置的升压电路，可通过FB脚设置升压值，以满足不同的输出功率需求。其还可通过外置电阻调节开关峰值电流限值。

此外，HT81696内部集成免滤波器调制技术，能够直接驱动扬声器，内置的关断功能使待机电流最小化，还集成了输出端过流保护、片内过温保护、输入电源欠压异常保护、升压电压过压保护等功能。

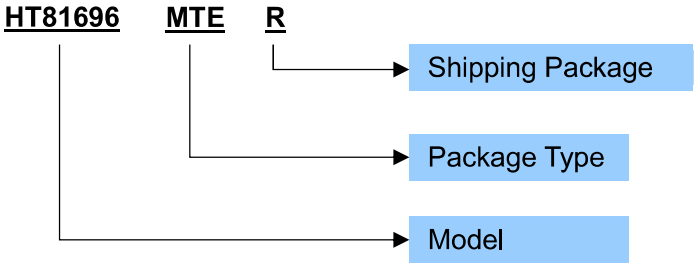
TYPICAL APPLICATION



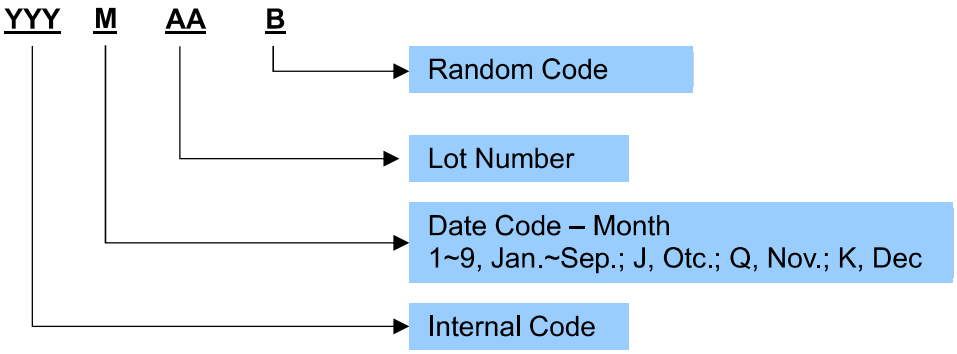
■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HT81696MTER	ETSSOP28	HT81696 YYYMAAB[1]	-40℃～85℃	Tape and Reel 3000PCS

Part Number

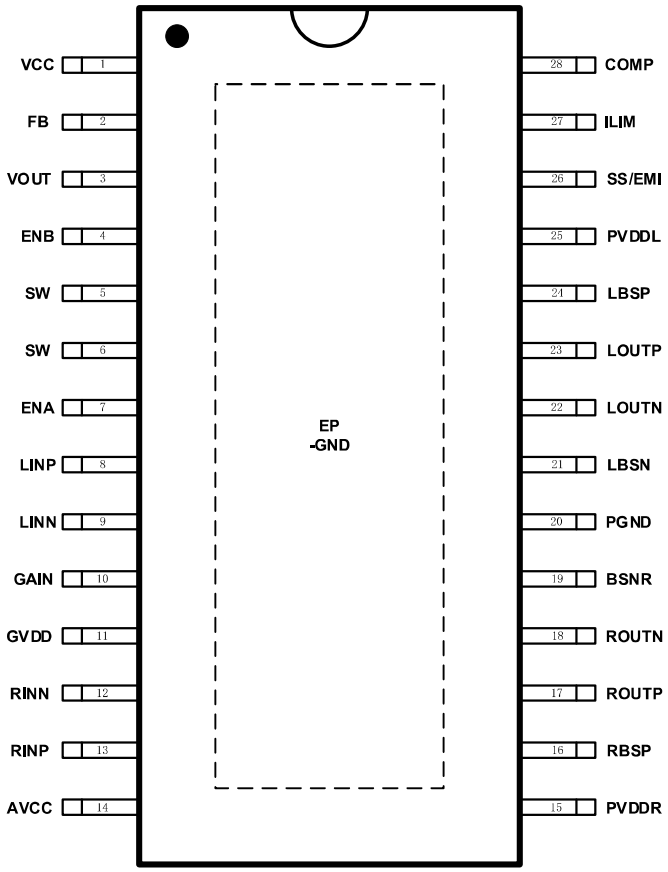


Production Tracking Code



[1] YYYMAAB is production tracking code

TERMINAL CONFIGURATION



Top View

TERMINAL FUNCTION

Terminal No.	Name	I/O[1]	Description
EP	GND	G	Ground. Also provides thermal connection from the device to the board. A matching ground pad should be provided on the PCB and the device connected to it via solder. 地，同时提供器件向板级散热的路径。PCB 板上需要留有足够的铺地露铜与之良好焊接。
1	VCC	O	Output of the internal regulator for boost converter. A ceramic capacitor of 1uF is required between this pin and ground. 升压电路内部电压输出，接 1uF 到底。
2	FB	I	Voltage feedback. 电压反馈脚
3	VOUT	P	Power supply for boost converter. 升压供电端
4	ENB	I	Enable logic input for boost converter. Logic high level enables the device. Logic low level disables the device and turns it into bypass mode. 升压使能脚，高电平时升压开启，低电平时升压关闭
5,6	SW	P	The switching node pin of the converter. 升压开关点

[1] I: Input; O: Output; G: Ground; P: Power

7	ENA	I	Enable logic input and operation mode selection for amplifier
8	LINP	I	Positive input (differential+) for audio amplifier of left channel. 音频左声道输入正端。
9	LINN	I	Negative input (differential-) for audio amplifier of left channel. 音频左声道输入负端。
10	GAIN	I	Gain select pin. Gain is 17.5dB when logic low, and 31.8dB when logic high or floating 增益选择。拉低时，增益 17.5dB；拉高或悬空时，增益 31.8dB
11	GVDD	O	Voltage regulator of amplifier, connect 1uF to GND. 功放内部电压，接 1uF 到地
12	RINN	I	Negative input (differential-) for audio amplifier of right channel. 音频右声道输入负端。
13	RINP	I	Positive input (differential+) for audio amplifier of right channel. 音频右声道输入正端
14	AVCC	P	Analog power supply for amplifier 功放模拟供电
15	PVDDR	O	Power supply terminal for right channel. 右声道功率电源端。
16	RBSP	BST	Connection point for the ROUTP bootstrap capacitor, which is used to create a power supply for the high-side gate drive for ROUTP. ROUTP 自举电容端
17	ROUTP	O	Positive output terminal (BTL+) for right channel. 右声道正端输出
18	ROUTN	O	Negative output terminal (BTL-) for right channel. 右声道负端输出。
19	RBSN	BST	Connection point for the ROUTN bootstrap capacitor, which is used to create a power supply for the high-side gate drive for ROUTN. ROUTN 自举电容端
20	PGND	P	Power ground for amplifier 功放功率地
21	LBSN	BST	Connection point for the LOUTN bootstrap capacitor, which is used to create a power supply for the high-side gate drive for LOUTN. LOUTN 自举电容端
22	LOUTN	O	Negative output terminal (BTL-) for left channel. 左声道负端输出。
23	LOUTP	O	Positive output terminal (BTL+) for left channel. 左声道正端输出。
24	LBSP	BST	Connection point for the LOUTP bootstrap capacitor, which is used to create a power supply for the high-side gate drive for LOUTP. LOUTP 自举电容端
25	PVDDL	P	Power supply terminal for left channel. 左声道功率电源端。
26	SS	O	Soft-start programming pin. An external capacitor connected to ground sets the ramp rate of the internal error amplifier's reference voltage during soft-start. 升压软启动设置脚，接电容到地。 Also used as mode selection for different tr/tf, an external resistor connected to ground selects a flatter tr/tf. 同时作为 tr/tf 设置脚，当同时外接 1 个 330k 电阻到地时，选择较缓的 tr/tf。
27	ILIM	I	Adjustable switch peak current limit. An external resistor should be connected between this pin and GND. 最大限流值设置端，外部接电阻到地。
28	COMP	O	Output of the internal error amplifier, the loop compensation network should be connected between this pin and the AGND pin. 内部补偿脚

SPECIFICATIONS[1]

Absolute Maximum Ratings[2]

PARAMETER		Symbol	MIN	MAX	UNIT
Voltage range	VOUT, PVDD, AVDD	V_{IN}	-0.3	18	V
	SW	V_{SW}	-0.3	22	V
	LINP, LINN, RINP, RINN, ENA	V_I	-0.3	5.8	V
	ENB, VCC, SS, COMP	V_I	-0.3	7	V
	ILIM, FB	V_I	-0.3	3.6	V
Operating temperature range		T_A	-40	85	℃
Operating junction temperature range		T_J	-40	150	℃
Storage temperature range		T_{STG}	-50	150	℃

Recommended Operating Condition

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
VBAT supply voltage range	V_{IN}		2.7	3.7	15	V
Output voltage range (VOUT, AVDD, PVDD)	V_{OUT}		4.5		15	V
High-level input voltage of ENA, spread spectrum enabled	V_{ENAH}		2.5		5.5	V
Middle-level input voltage of ENA, spread spectrum disabled	V_{ENAM}		1.7		2.1	V
Low-level input voltage of ENA, amplifier shutdown	V_{ENAL}		0	0	0.8	V
High-level input voltage of ENB	V_{ENBH}		1.5		5.5	V
Low-level input voltage of ENB	V_{ENBL}		0		0.4	V
ENB internal pull-down resistor	R_{ENB}			800		kΩ
Inductance	L		1		10	μH
Operating temperature	T_a		-40	25	85	℃
Load impedance	R_L		3.2			Ω

Electrical Characteristics

Boost Converter

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Output voltage range	V_{OUT}		4.5		15	V
Output overvoltage protection	V_{OVP}			18		V
Under-voltage lockout (UVLO) threshold for VOUT	V_{UVLO}	Rising		2.7		V
		Falling		2.5		V
Reference voltage at the FB pin	V_{FB}			1.204		V
Soft-start charging current	I_{SS}			5		uA
VCC regulation	VCC	V_{BAT} = 3.6V, V_{OUT} = 12V, light load		5.7		V
		V_{BAT} = 3.6V, V_{OUT} = 12V, I_{LOAD} = 0.5A		5.3		V
Boost converter input current limit	I_L	R_{ILIM} = 130k		13		A
Boost converter frequency	f_{BOOST}	R_{FREQ} = 330k, VIN = 3.7V, VOUT = 12V		360		kHz

Audio Amplifier

[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Amplifier Output Offset Voltage	V_{OS}	V_I = 0V, Gain = 32dB		1.5		mV
Quiescent supply current in SD mode	I_{SD}	V_{BAT} = 3.7V		11		uA
		V_{BAT} = 7.4V		24		uA
Operating quiescent current	I_{BAT}	VBAT = 3.7V, PVDD = 9V, ENA=ENB=H		34		mA
		VBAT = 3.7V, PVDD = 12.5V, ENA=ENB=H		55		mA
		VBAT = 7.4V, PVDD = 16V, ENA=ENB=H		39		mA
		VBAT = 7.4V, PVDD = 12.5V, ENA=ENB=H		26		mA
System Gain	Gain	GAIN=H, Rin = 0kΩ		31.8		dB
		GAIN=H, Rin = 10kΩ		25.8		dB
		GAIN=L, Rin = 0kΩ		17.5		dB
Turn-on time	t_{on}			40		ms
Turn-off time	t_{off}	Pull \SD low		5		us
Total harmonic distortion plus noise	THD+N	P_O=0.25W, R_L=4Ω, f=1kHz		0.02		%
Noise output voltage	V_N	f=20Hz~20kHz, A-weighted, GAIN=L, RIN=0		75		μV_{rms}
		f=20Hz~20kHz, A-weighted, GAIN=H, RIN=10		130		μV_{rms}
Class D switching frequency	$f_{Class-D}$			360		kHz
Spread frequency range				±15		kHz
GVDD regulation	GVDD			5		V
Over current trip point	OCP			7.5		A

Boost Converter + Class D

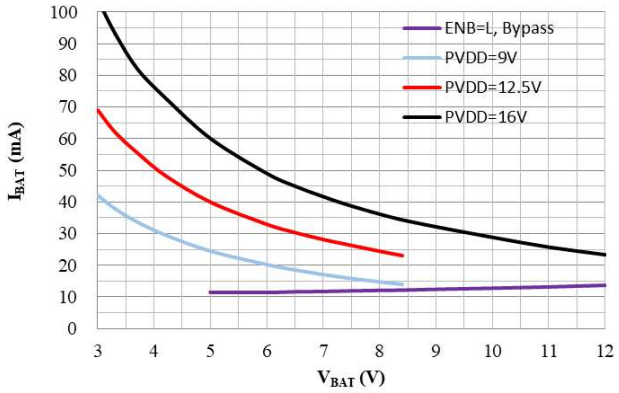
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Efficiency (Class D + Boost)	η	V_{BAT} = 4.2V, PVDD = 9V, R_L=4Ω, Po = 2×10W		80		%
		V_{BAT} =8.4V, PVDD = 14.8V R_L=4Ω, Po = 2×40W		82		
Thermal shutdown threshold	T_{SD}			150		℃
Thermal shutdown hysteresis	T_{SD_HYS}			20		℃

Power specifications

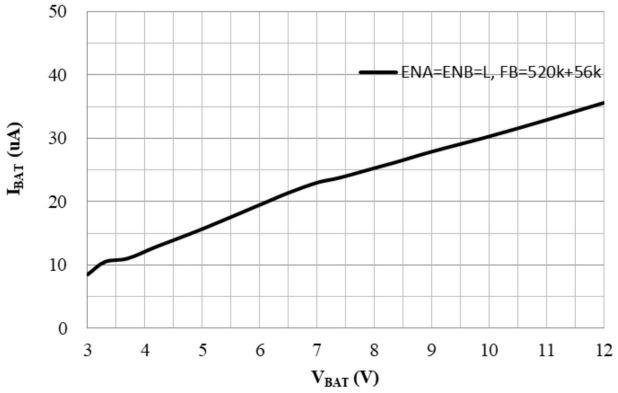
Condition		Power supply							UNIT
		3.3V	3.7V	4.2V	6.5V	7.2V	8.4V	12V	
Load=4ohm PVDD=14.8V	THD+N=1%				21.7	21.7	21.7	21.7	W
	THD+N=10%				22.6	25.6	26.6	26.6	W
Load=4ohm PVDD=12.5V	THD+N=1%				15.8	16.0	16.0	16.0	W
	THD+N=10%				20.0	20.0	20.0	20.0	W
Load=4ohm, PVDD=9V	THD+N=1%	8.2	8.2	8.2					W
	THD+N=10%	9.70	10.2	10.2					W

■ TYPICAL OPERATING CHARACTERISTICS

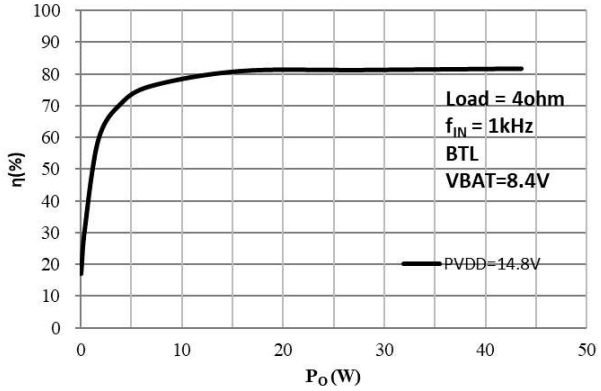
Quiescent Current



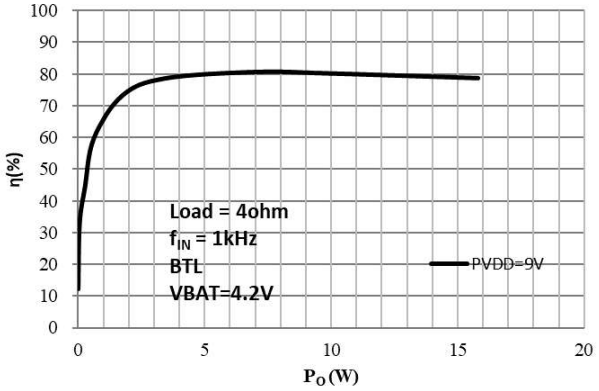
Shutdown Current

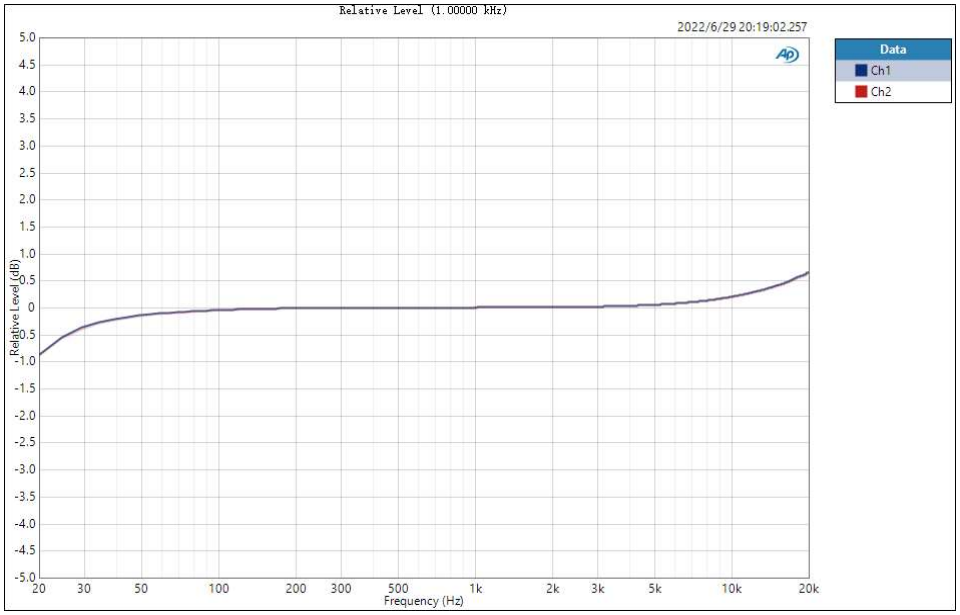


P_O vs η



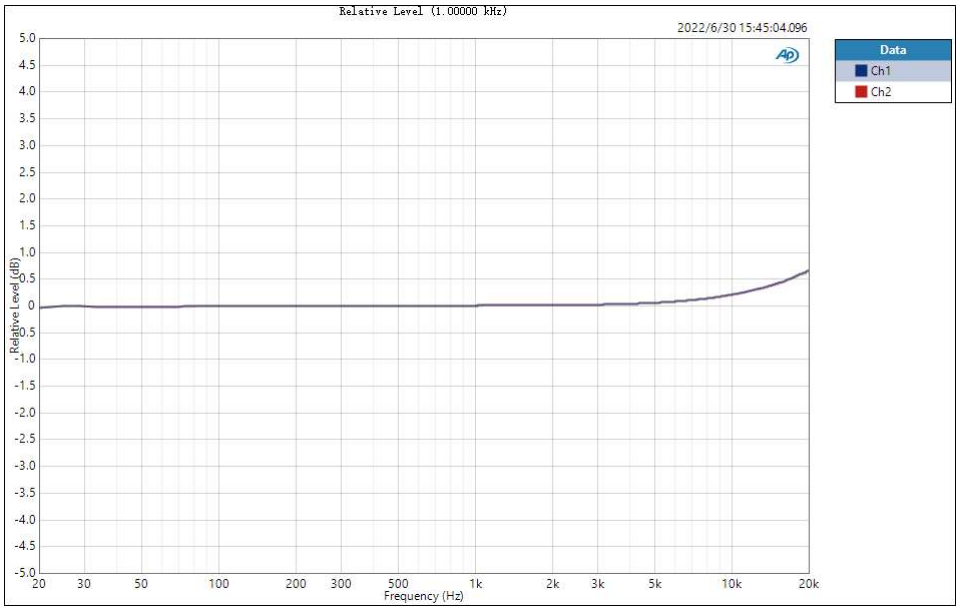
P_O vs η





Frequency respond

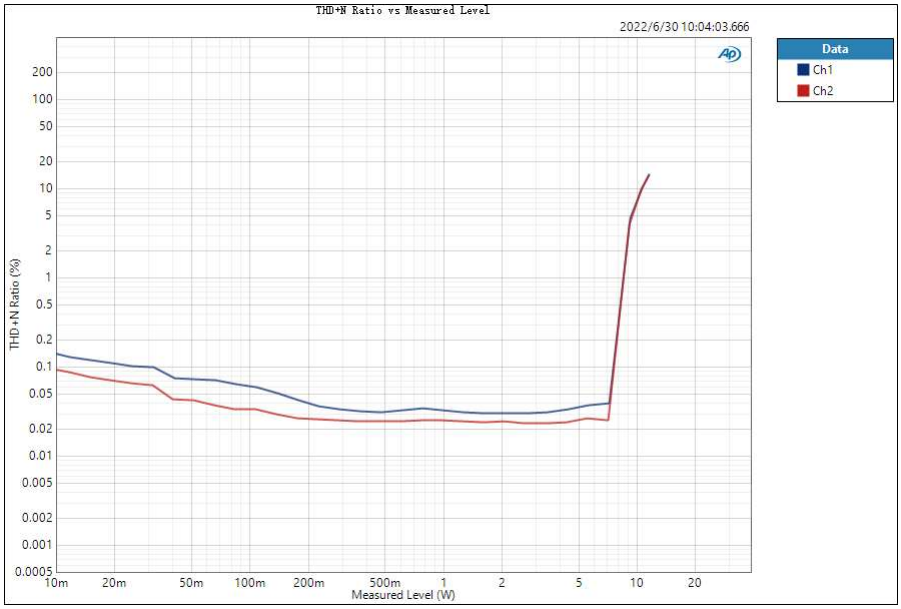
(Cin = 1uF, Rin=10k, Gain=H)



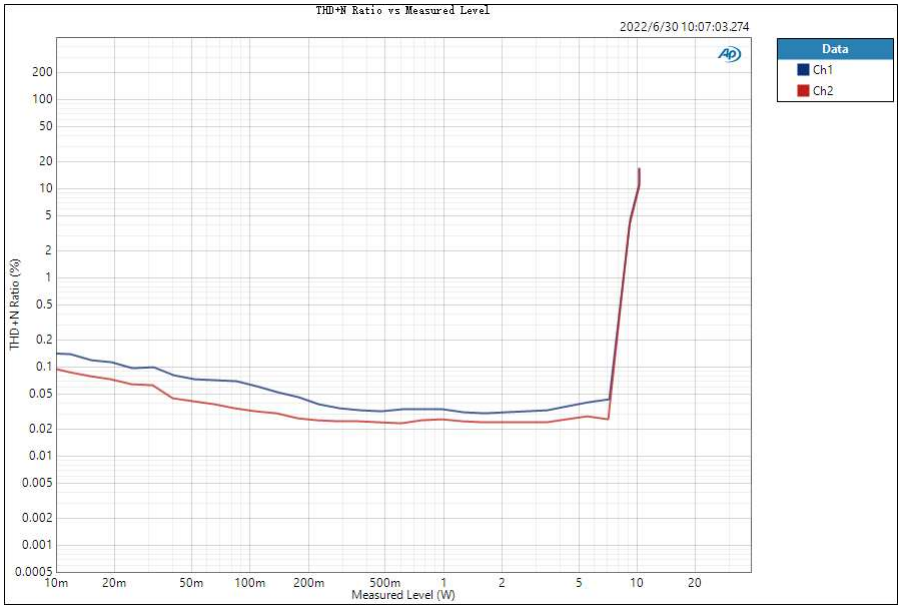
Frequency respond

(Cin = 1uF, Rin=0k, Gain=L)

RL = 4ohm, f_{IN} = 1kHz, VBAT = 4.2V, PVDD=9V, R_{ILIM} = 130k, unless otherwise specified.

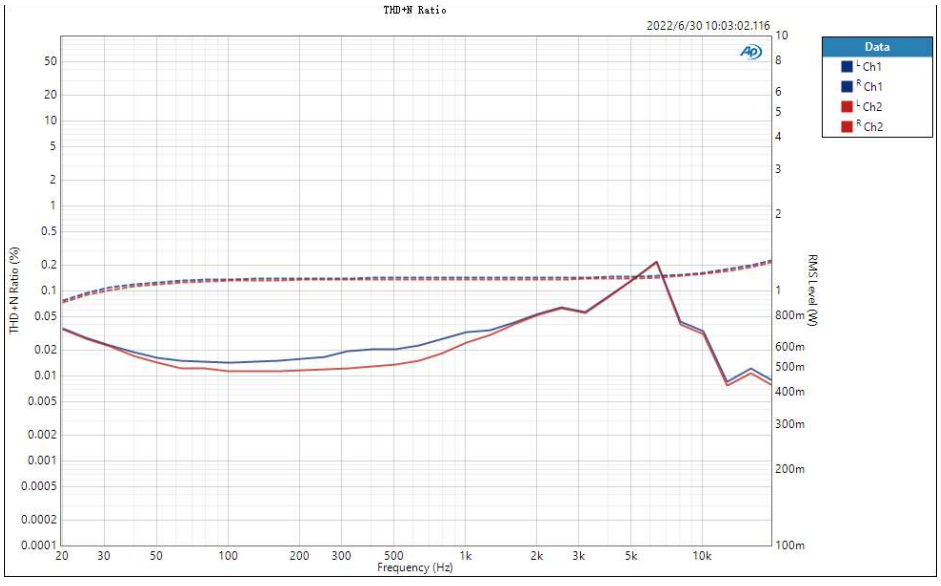


Output power vs THD+N



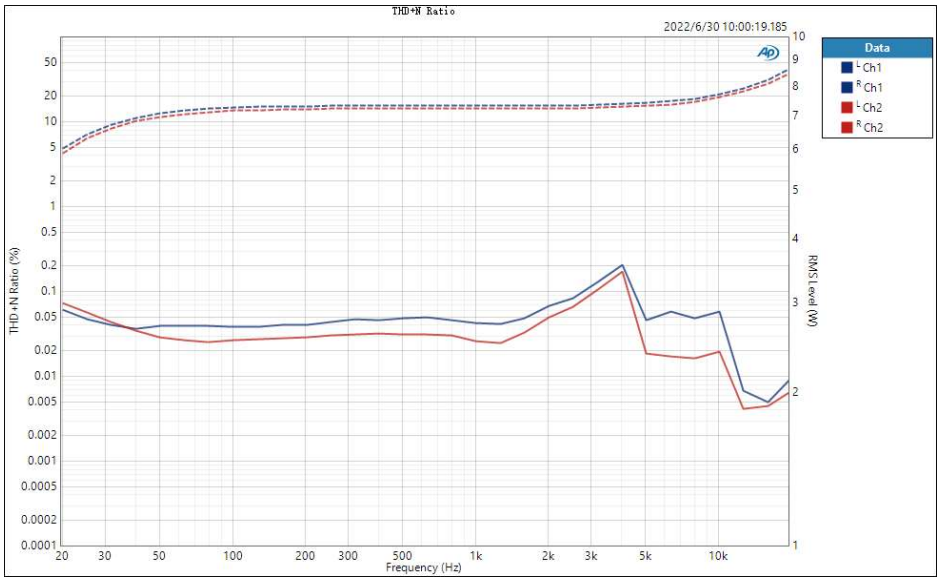
Output power vs THD+N

VBAT = 3.3V



frequency vs THD+N

(Po ≈ 2×1W)



frequency vs THD+N

(Po ≈ 2×7.5W)

APPLICATION INFORMATION

1. Boost Converter

The integrated boost converter operates at a quasi-constant frequency pulse width modulation (PWM) in moderate to heavy load condition. The boost converter improves the efficiency at light load with the PFM mode.

HT81696 内置升压，在非轻载时，工作在近固定频率的 PWM 调制方式。轻载时，则工作在 PFM 模式。

1.1 Enable and Startup (ENB and SS pin)

The 81696 has an adjustable soft start function to prevent high inrush current during start-up. To minimize the inrush current during start-up, an external capacitor, connected to the SS pin and charged with a constant current, is used to slowly ramp up the internal positive input of the error amplifier. The larger the capacitance at the SS pin, the slower the ramp of the output voltage and the longer the soft-start time. A 1uF capacitor is usually sufficient for most applications.

HT81696 integrates two modes with different tr/tf. With a single capacitor (C_{SS}) connected betweeen SS/EMI pin and Ground, the mode with steep tr/tf will be selected, HT81696 operates with a higher efficiency and poorer EMI performance. However, if a capacitor (C_{SS}) paralleled with a resistor 330k (R_{EMI}) is placed between SS/EMI pin and Ground, the mode with flatter tr/tf is selected, HT81696 operates with a lower efficiency and better EMI performance.

When the ENB pin is pulled into logic low (below 0.4V), the boost converter stops switching and goes into bypass mode (the amplifier power is powered directly by input power supply through Schottky diode).

Only when ENB pin is pulled into logic high (above 1.5V), the boost converter works.

HT81696 具有软启动功能，以避免启动过程中的冲击电流。SS 外接电容，可调节软启动时间，电容越大，软启动时间越长。通常情况下，1uF 电容可满足要求。

HT81696 具有两种不同 tr/tf 时间的模式。当 SS/EMI 引脚仅接一个电容(C_{SS})到地时，tr/tf 更陡，此时 HT81696 的效率更高，但 EMI 表现更差；当 SS/EMI 引脚接一个电容(C_{SS})并联 330k 电阻到地时，tr/tf 更缓，此时 HT81696 的效率更低，但 EMI 表现更好。

当 ENB 拉低（小于 0.4V）时，升压关闭，进入直通模式，功放供电由输入电压经肖特基二极管直接供电。

当 ENB 高于 1.5V 时，升压工作。

1.2 Adjustable Peak Current Limit (ILIM pin)

To avoid an accidental large peak current, an internal cycle-by-cycle current limit is adopted. The low-side switch is turned off immediately as soon as the switch current touches the limit. The peak switch current limit can be set by a resistor (R_{ILIM}) at the ILIM pin to ground. The relationship between the current limit and the resistance is as the following equation, or figure. The current limit should be set lower than 14A.

$$I_{LIM} = 1338 \times \left(\frac{R_{ILIM}}{1k}\right)^{-0.95}$$

为了避免意外的尖峰电流，HT81696 具有逐周期限流功能。当开关电流达到限流值后，低端管迅速关闭。开关管限流值可通过 ILIM 脚的接地电阻 R_{ILIM} 调节，如下公式或曲线图。峰值电流限制值设置应小于 14A。

$$I_{LIM} = 1338 \times \left(\frac{R_{ILIM}}{1k}\right)^{-0.95}$$

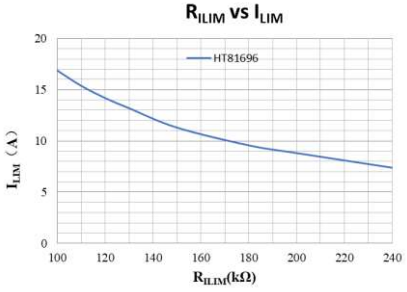


Figure 1 Peak Current Limit (ILIM) vs ILIM terminal resistor (R_{ILIM})

1.3 Output Voltage Setting (FB pin)

The output voltage is set by an external resistor divider (R_{UP}, R_{DN} in the Typical Application Circuit). To get the output voltage V_{OUT}, the Value of R_{UP} and R_{DN} can be calculated as:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{UP}}{R_{DN}})$$

Where V_{REF} = 1.204V.

Some typical output voltages can be set as the following parameters.

输出电压 V_{OUT} 可通过 FB 的上下拉电阻 R_{UP}, R_{DN} 调节：

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{UP}}{R_{DN}})$$

其中，V_{REF} = 1.204V

典型电压设置如下。

V_{OUT}(V)	R_{UP}(Ω)	R_{DN}(Ω)
7.4	510k	100k
9	520k	82k
12.5	520k	56k
14.8	510k	47k

1.4 Inductor Selection (SW pin)

Because the selection of the inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

To be simplified, the inductor value can be set as 2.2uH or 4.7uH which can be used in most cases.

The rated current, especially the saturation current should be larger than the peak current during the whole operation. The peak current can be calculated as follows:

升压电感的选型，直接影响到系统的运行稳定性。电感选型最重要的三个参数：电感值，DCR，饱和电流。

简单来说，电感值可选择 2.2uH 或 4.7uH，可满足大多数应用条件。

电感的额定电流、特别是饱和电流，必须大于整个运行条件下的最高峰值电流。峰值电流可如下计算：

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2}$$

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}}$$

Boost converter efficiency is affected significantly by the inductor's DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. An inductor with lower DCR and ESR would increase the efficiency significantly.

The inductor should be placed as close as possible to the SW pin. For a lower EMI radiation, connecting a resistor Rsw (Typ. 1ohm) and a capacitor Csw (Typ. 3.3nF) in series from SW to the ground, and also a resistor Rsw (Typ. 1ohm) and a capacitor Csw (Typ. 1nF) in series from SW to the output voltage terminal (the cathode of Schottky diode) would be helpful.

升压效率受电感的DCR、开关频率下的等效ESR、以及铁损影响较大。使用较低的DCR和ESR的电感，可提高整体效率。

电感应尽可能靠近 SW 脚防止。SW 脚串接一个电阻和电容（典型值 1ohm 和 3.3nF）到地，SW 脚串接一个电阻和电容（典型值 1ohm 和 1nF）到升压输出端（肖特基二极管阴极）可有效降低芯片的 EMI 辐射。

1.5 Input and Output Capacitor Selection (V_{BAT}, VCC, GVDD, AVCC, VOUT, PVDD pin)

For good input voltage filtering and small voltage ripple (less than 100mV is required), we recommend low-ESR capacitors of 10uF//220uF ("//" represents paralleled) be placed as close as possible to the inductor (VBAT).

The VOUT pin is the power supply for boost converter, the AVCC pin is the analog power supply for amplifier, a 1uF should be placed as close as possible to them.

The VCC and GVDD pin is the output of internal LDO. A ceramic capacitor of 1uF is required at VCC and GVDD pin to get a stable operation of LDO.

To be simplified, we recommend low-ESR capacitors of 0.1uF//1uF//220uF ("//" represents paralleled) be placed as close as possible to the output terminal of boost converter (Schottky diode) .

Capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

为了输入电压的稳定性和良好滤波，建议在电压输入端（VBAT）加入 10uF//220uF 的并联电容到地。

VOUT 和 AVCC 脚分别是升压电路的供电电压和功放模拟供电，建议各放置 1uF 电容。

VCC 和 GVDD 脚是内部的一个 LDO 输出，需各自连接一个 1uF 电容到地。

升压输出电压端(肖特基二极管端)，建议放置 0.1uF//1uF//220uF 的并联电容到地，电容的额定电压需留有足够的余量。

1.6 6.4 Loop Stability (COMP pin)

The boost converter requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network comprised of resister R_C, ceramic capacitors C_C and C_P is connected to the COMP pin.

HT81696需要外部补偿电路，以使不同应用下环路响应得到优化。补偿电路是COMP脚外接的 R_C、C_C和 C_P。

To be simplified, RC is 33kΩ, CC is 3.3nF, and CP is 150pF. But notice that this setting can only be adopted in most cases. In detail, the compensation network parameters can be calculated as follows.

(1) Set the cross over frequency, f_c

The first step is to set the loop crossover frequency, f_C. The higher crossover frequency, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. It's proper to use a fixed parameter of 10kHz for f_C.

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L}$$

(2) Set the compensation resistor, R_C.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{sense} \times f_C \times C_O}{(1-D) \times V_{REF} \times G_{EA}}$$

(3) Set the compensation zero capacitor, C_C

$$C_C = \frac{R_O \times C_O}{2 \times R_C}$$

(4) Set the compensation pole capacitor, C_P

$$C_P = \frac{R_{ESR} \times C_O}{R_C}$$

If the C_P is less than 10pF, it can be left open.

• R_O is the output load resistance.

• D is the switching duty cycle. 1 - D = V_{IN} / V_{OUT}

• R_{sense} is the equivalent internal current sense resistor, which is 0.084 Ω.

• C_O is output capacitor.

• V_{REF} is the reference voltage at the FB pin, which is 1.204V.

• G_{EA} is the amplifier's transconductance, which is 190uA/V.

• R_{ESR} is the equivalent series resistance of the output capacitor.

通常情况下，R_C 33k、C_C 3.3nF C_P 150pF可满足应用，但仍可能存在不适用的情况。具体的，补偿电路参数可按照如下步骤设置。

（1） 设置交叉频率 fc

交叉频率越高，环路响应越快。一般其取 1/10 f_{sw}，或 1/5 f_{RHPZ}，或固定的 10kHz。

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L}$$

（2） 设置 Rc

$$R_C = \frac{2\pi \times V_{OUT} \times R_{sense} \times f_C \times C_O}{(1-D) \times V_{REF} \times G_{EA}}$$

（3） 设置 Cc

$$C_C = \frac{R_O \times C_O}{2 \times R_C}$$

（4） 设置 Cp

$$C_P = \frac{R_{ESR} \times C_O}{R_C}$$

如果 Cp 小于 10pF，其可以悬空。

其中:

Ro 是输出等效负载阻值；

D开关占空比， 1 - D = V_{IN} / V_{OUT}

R_{sense} 是内部等效感流电阻，为 0.084 Ω

Co 是输出电容；

V_{REF} 是 FB 电压，为 1.204V;

G_{EA} 是跨导，为 190uA/V；

R_{ESR} 是输出电容的等效串联电阻。

1.7 Schottky Diode selection

Schottky diode with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

肖特基二极管应选择快恢复时间和低正向电压。应确保二极管的平均额定电流、峰值额定电流超过输出平均电流和电感峰值电流。此外，二极管的反向击穿电压应大于输出电压。

2. Class D Audio Amplifier

The integrated audio power amplifier operates at Class D operation. The power supply of the amplifier (PVDDR and PVDDL) is supplied from the output voltage of the boost converter. Therefore, PVDDR and PVDDL should be connected to VOUT. The PVDDL feeds the power stage of L channel and the PVDDR feeds the power stage of R channel. Filtering capacitors of 100nF//1uF//220uF for PVDD of each channel should be placed close to the PVDD pin.

The GVDD pin is the output of internal LDO. A ceramic capacitor of 1uF is required at the VCC pin to get a stable operation of LDO.

HT81696内置的D类音频功放，由升压后的电压供电，因此PVDDL和PVDDR需要连接至VOUT。PVDDL是功放左通道的电源，PVDDR是功放右通道的电源，建议分别加100nF//1uF//220uF的并联滤波电容到地。

GVDD是内部的LDO输出，建议加1uF电容到地。

2.1 Amplifier Input Configuration

HT81696 integrates an amplifier with analog input (single-ended or differential). For a differential operation, input signals into IN+ and IN- pins via DC-cut capacitors (C_{IN}). The high pass cut-off frequency of input signal can be calculated by

$$f_c = \frac{1}{2\pi(External\ R_{IN} + Internal\ R_{IN}) \times C_{IN}}$$

The input signal gain is calculated by

$$Gain = 20 \times \log\left(\frac{R_F}{External\ R_{IN} + Internal\ R_{IN}}\right).$$

When Gain = H, The internal R_F=390k, internal Rin=10k; When Gain = L, The internal R_F=390k, internal Rin=52k.

For a single-ended operation, input signals to IN+ pin via a DC-cut capacitor (C_{IN}). IN- pin should be connected to ground via a DC-cut capacitor (with the same value of C_{IN}).

HT81696 支持差分输入或单端输入。

差分输入时，信号经过输入隔直电容 C_{IN} 连接到 IN+和 IN-，高通滤波器截止频率为：

$$f_c = \frac{1}{2\pi(External\ R_{IN} + Internal\ R_{IN}) \times C_{IN}}$$

放大倍数为：

$$Gain = 20 \times \log\left(\frac{R_F}{External\ R_{IN} + Internal\ R_{IN}}\right)$$

当 Gain 拉高时，internal R_F=390k, internal Rin=10k;
当 Gain 拉低时, The internal RF=390k, internal Rin=52k。

单端输入时，信号经输入隔直电容 C_{IN} 连接至 IN+, IN-接相同的输入电容到地。

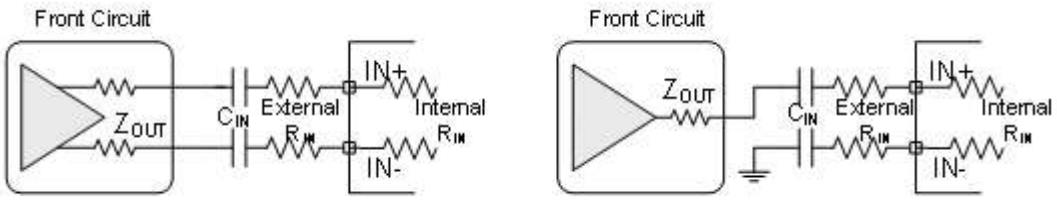


Figure 2 (1) Differential Input; (2) Single-ended Input

2.2 Amplifier Output Configuration

The HT81696 can be used with a simple ferrite bead filter for some applications. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the class-D amplifier. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz. Also, the filter capacitor can be increased if necessary, with some impact on efficiency.

HT81696在部分应用场合，可使用磁珠作为滤波器。对于磁珠的选择，不同材料类型会有不同的表现，关键之一是在10M ~ 100MHz内表现。使用磁珠时，可配合使用1nF的下地电容，谐振频率应小于10MHz。

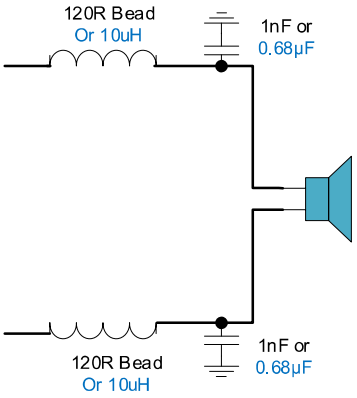


Figure 3 Output Filters Configurations

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in the figures below can be used.

在某些条件下，如周边元器件对辐射较为敏感，或EMI辐射难以达到标准，输出需要加LC滤波器。

2.4 Shutdown

The HT81696 employs a shutdown mode of operation designed to reduce supply current (IDD) to the absolute minimum level during periods of nonuse for power conservation. The ENA input terminal should be held high during normal operation when the amplifier is in use. Pulling ENA low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave ENA unconnected and pull \SD down less than 100us, because amplifier operation would be unpredictable.

For a better power on and power-off pop performance, place the amplifier in the shutdown mode prior to delivering or removing the power supply.

To be simplified, ENA and ENB can be connected to logic high or logic low. When logic high, the whole chip works. And when logic low, the whole chop shutdown.

HT81696具有关断功能，以使芯片进入低功耗状态。当ENA拉高时，芯片进入工作状态；当ENA拉低时，芯片进入关断状态。

ENA不建议悬空，也不建议\SD低电平的状态小于100us，否则可能状态不定。

上下电时，为减小pop声，在上、下电前，将功放关闭进入关断状态。

为方便控制，ENA和ENB可以短接在一起控制，此时拉高，芯片全部工作；此时拉低，芯片全部关闭。

2.5 Spread Spectrum

The HT81696 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM outputs to improve EMI performance. The spread spectrum scheme is internally fixed and by setting the ENA pin above 2.5V to turn on.

HT81696具有扩频功能，以提升EMI表现。当关断功能，以使芯片进入低功耗状态。当ENA电压高于2.5V时，该功能开启。

3. Protection Functions

3.1 Over Temperature Protection (OTP)

When the on-die temperature of HT81696 is higher than 150℃, the OTP mode is activated, the differential output pin becomes weak low state (a state grounded though resistivity), the boost converter stops switching and the ENA pin is pulled low. When the one-die temperature falls below typically 130°C, the device start working again.

HT81696内部高于150℃时，芯片OTP保护功能启动，功放关断、升压停止开关、ENA拉低。此后，芯片低于130℃后，芯片重新恢复工作。

3.2 DC Detect Protection (DCP)

The HT81696 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. A DC detect fault will pull ENA low. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2 Hz.

HT81696具有直流保护功能，以保护可能的喇叭端直流信号。保护功能发生时，ENA拉低，功放关断。

当输出某个通道的差分信号在同一极性的占空比超过60%并持续429ms以上，直流保护功能开启。

3.3 Short-Circuit Protection (OCP)

The HT81696 has protection from over current conditions caused by a short circuit on the output stage. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The short circuit protection fault is reported on the ENA pin as a low state.

When OCP or OTP or DCP error is detected, the ENA pin will be pulled low. After a delay time (typically 1.3s), HT81696 will try restart.

当HT81696输出短路而发生过流时，芯片会发生保护，芯片关断，ENA拉低。

当OCP, OTP, DCP发生时，ENA均会被拉低，经过1.3s, HT81696会尝试重新启动。

3.4 Under-Voltage Protection (UVP)

The UVP circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The HT81696 has both VOUT UVP function and VCC UVP function. It disables the device from switching when the falling voltage at the VINB pin trips the UVP threshold typically 2.4V. The device starts operating when the rising voltage at the VINB pin is above 2.6V. It also disables the device when the falling voltage at the VCC pin trips typically 2.1V

HT81696具有欠压保护功能，以防止输入电压过低。

当VOUT小于2.4V时，欠压保护启动，升压关闭。当VINB高于2.7V时，升压重新开启。

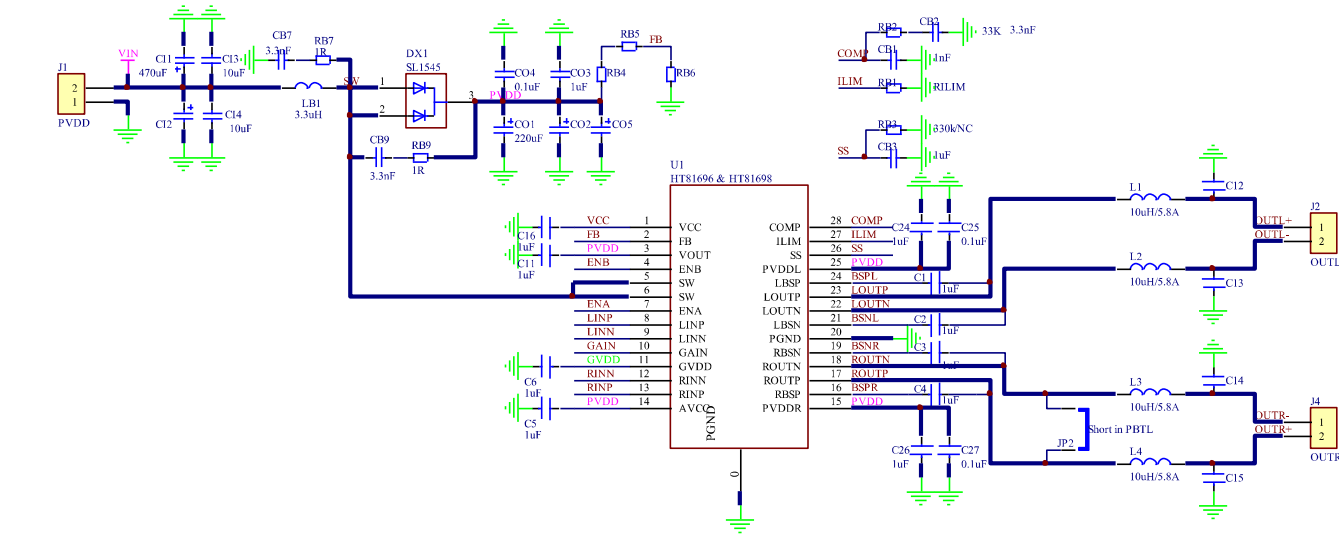
当VCC电压低于2.1V时，升压同样关闭。

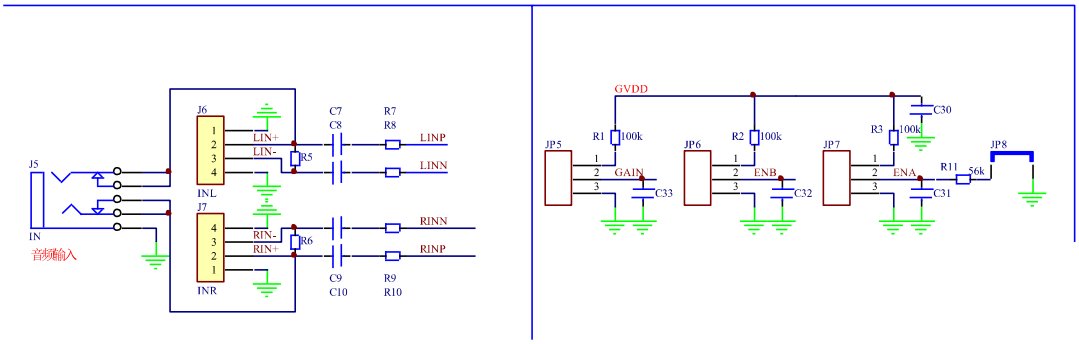
3.5 Over-Voltage Protection (OVP)

The HT81696 device monitors the voltage on VOUT. If the output voltage at the VOUT pin is detected above 18V (typical value), the boost converter stops switching immediately until the voltage at the VOUT pin drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

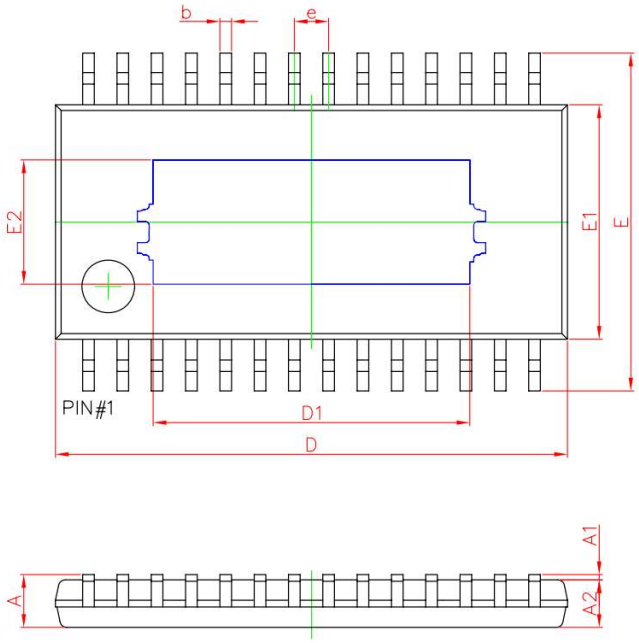
HT81696检测VOUT电压，当升压输出VOUT检测到高于18V时，升压关闭，直到VOUT电压降低。

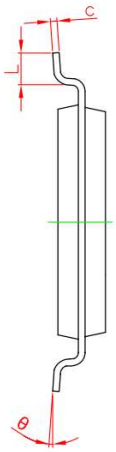
4. *Typical Circuit Diagram*





■ PACKAGE OUTLINE





Symbol	Dimensions In Millimeters	
	Min	**Max**
A	——	1.200
A1	0	0.1
A2	0.800	1.050
b	0.190	0.300
c	0.090	0.200
D	9.600	9.800
D1	5.908	6.108
E	6.250	6.550
E1	4.300	4.500
E2	2.253	2.453
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°